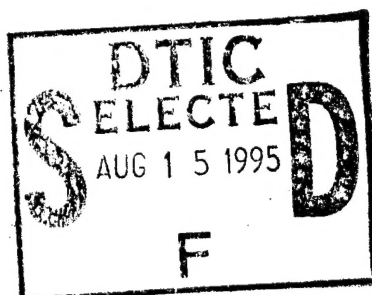


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OHMIC CONTACT TO ION IMPLANTED GALLIUM
ARSENIDE ANTIMONIDE FOR APPLICATION TO
INDIUM ALUMINUM ARSENIDE/GALLIUM
ARSENIDE ANTIMONIDE HETEROSTRUCTURE
INSULATED-GATE FIELD EFFECT TRANSISTORS

DISSERTATION

Kenneth G. Merkel II, Captain, USAF

AFIT/DSG/ENG/95S-03

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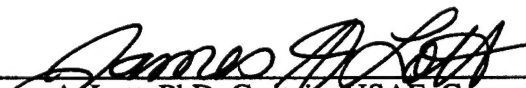
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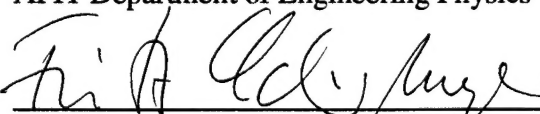
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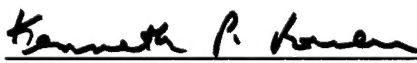
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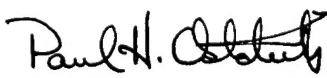
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ANTIMONIDE HETEROSTRUCTURE INSULATED-GATE FIELD EFFECT
TRANSISTORS

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Presented to the Faculty of the Graduate School of Engineering
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Air Education and Training Command
In Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

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List of Symbols

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
ϕ_m	Metal work function	energy	electron-volt	2.1
χ	Electron affinity	energy	electron-volt	2.1
E_m	Fermi level in metal	energy	electron-volt	2.1
E_{Fn}	Fermi level in n-type semiconductor	energy	electron-volt	2.1
δ	Metal-semiconductor separation distance	length	angstrom	2.1
E_c, E_v	Conduction, valence band energy level	energy	electron-volt	2.1
W	Depletion layer width	length	angstrom	2.1
	Tungsten element	n/a	n/a	2.2
	Electrical contact width	length	micrometer	2.4
ϕ_B	Metal-semiconductor barrier height	energy	electron-volt	2.1
V_{bi}	Built-in potential	electromotive force	volt	2.1
V_A	Applied potential	electromotive force	volt	2.1
$\psi(x)$	Electrostatic potential	electromotive force	volt	2.1
ϵ_s	Semiconductor static dielectric permittivity	capacitance/length	farad/centimeter	2.1
ρ	Charge density	electric flux/volume	coulomb/cubic centimeter	2.1
q	Electron charge	electric flux	coulomb	2.1
k	Boltzmann constant	energy/temperature	electron-volt/Kelvin	2.1
T	Temperature	temperature	Kelvin	2.1

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
N_D, N_A	Donor, acceptor concentration	atom/volume	atoms/cubic centimeter	2.1
ρ_c	Specific contact resistance	resistance-area	ohm-square centimeter	2.1
J	Current density	current/area	ampere/square centimeter	2.1
E_{00}	Characteristic energy	energy	electron-volt	2.1
A^*	Richardson constant	current/(temp*area)	ampere/Kelvin*square cm	2.1
A^{**}	Effective Richardson constant	current/(temp*area)	ampere/Kelvin*square cm	6.3
h	Planck constant	energy-time	electron-volt-second	2.1
m^*	Effective mass	mass	kilogram	2.1
E_p	Peak electron energy distribution	energy	electron-volt	2.1
m_e^*, m_h^*	Electron, hole effective mass	mass	kilogram	2.1
E_g	Band gap energy	energy	electron-volt	2.1
$\Delta\phi_{im}$	Image force lowering	energy	electron-volt	2.1
ϕ_{Bn}	Metal/n-semiconductor barrier height	energy	electron-volt	2.1
E_m	Maximum electric field	voltage/length	volt/centimeter	2.1
m_0	Electron rest mass	mass	kilogram	2.1
R_c	Contact resistance	electrical resistance	ohm or ohm-millimeter	2.2
R_T	Total resistance	electrical resistance	ohm	2.2

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
ρ	Electrical resistivity	electrical resistance-length	ohm-centimeter	2.2
L_T	Transfer length	length	micrometer	2.2
L	Electrical channel length	length	micrometer	2.2
	Depth from surface	length	angstrom	5.3
d	Electrical contact width	length	micrometer	2.2
R_{sh}	Sheet resistance	electrical resistance/area	ohm/square	2.2
R', G'	Resistance/conductance per unit length	electrical resistance or conductance/length	ohm or mho/micron	2.2
R_{sh1}	Sheet resistance under metal contact	electrical resistance/area	ohm/square	2.2
R_{sh2}	Semiconductor sheet resistance between metal contacts	electrical resistance/area	ohm/square	2.2
L_x	Zero resistance intercept length	length	micrometer	2.2
R_E	End resistance	electrical resistance	ohm	2.2
$V_{n_{ins}}, V_{p_{ins}}$	n, p channel insulated-gate layer voltage drop	electromotive force	volt	3.1
V_G	Applied gate voltage	electromotive force	volt	3.1
V_{tn}, V_{tp}	n, p channel threshold voltage	electromotive force	volt	3.1
ϕ_n, ϕ_p	n, p channel gate barrier voltage	electromotive force	volt	3.1

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
$\Delta E_C, \Delta E_V$	Conduction, valence band offset energy	energy	electron-volt	3.1
$V(0)$	Fermi-level to conduction or valence band voltage offset	electromotive force	volt	3.1
R_S, R_D	Source, drain resistance	electrical resistance	ohm	3.1
f_t	Unity current gain frequency	time ⁻¹	Gigahertz	3.1
g_m	Intrinsic transconductance	electrical conductance	millisemen/millimeter	3.1
C_{gs}, C_{gd}	Gate-source, gate-drain capacitance	capacitance	picofarad/millimeter	3.1
f_{max}	Maximum oscillation frequency	time ⁻¹	Gigahertz	3.1
r_{ds}	Small signal, differential output resistance	electrical resistance	ohm	3.1
R_i	Gate to channel resistance	electrical resistance	ohm	3.1
R_g	Gate contact resistance	electrical resistance	ohm	3.1
α	Varshni coefficient	energy/ temperature	electron-volt/Kelvin	4.3
β	Varshni coefficient	temperature	Kelvin	4.3
I_{ex}	Excitation intensity	energy/area	Watt/ square centimeter	4.3
E_D, E_A	Donor, acceptor ionization energy	energy	millielectron-volt	4.3
$E_{(D,A)}$	Donor-to-acceptor transition energy	energy	millielectron-volt	4.3

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
E_0	Energy-shift coefficient	energy	millielectron-volt	4.3
N_{DD}, N_{DA}	Deep donor, acceptor concentration	atom/volume	atoms/ cubic centimeter	4.4
ϕ_{sb}	Semiconductor surface Schottky barrier height	energy	electron-volt	4.4
$u_i(x)$	Electron/hole wave function	none	none	4.4
E_i	Schrödinger equation energy eigenvalues	energy	electron-volt	4.4
$V(x)$	Potential energy	energy	electron-volt	4.4
m_{hh}^*, m_{lh}^*	Heavy hole and light hole effective mass	mass	kilogram	4.4
$h(x)$	Normalized Pearson Distribution	none	none	5.2
R_p	Range	length	angstrom	5.2
ΔR_p	Straggle	length	angstrom	5.2
γ_1	Skewness	none	none	5.2
β	Kurtosis	none	none	5.2
$n(x)$	Implant concentration profile	atoms/volume	atoms/ cubic centimeter	5.2
Q_0	Implant dose	atoms/area	atoms/ square centimeter	5.2
R	Semiconductor bulk series resistance	electrical resistance	ohm	5.4
C	Depletion layer capacitance	capacitance	nanofarad	5.4
N	Measured atomic concentration	atom/volume	atom/ cubic centimeter	5.4

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
W_E	Etch depth	length	angstrom	5.4
M	Molecular weight	weight	atomic mass unit	5.4
η	Charge carriers/molecule	charge	coulomb	5.4
F	Faraday	charge	9.64×10^4 coulomb	5.4
D	Semiconductor density	mass density	gram/cubic centimeter	5.4
h_c	Critical thickness	length	angstrom	5.5
$a_o(x), a_o$	Unit cell length	length	angstrom	5.5
$f(x)$	Lattice mismatch	none	none	5.5
$\nu(x)$	Poisson's ratio	none	none	5.5
$c_{11}(x), c_{12}(x)$ $c_{44}(x)$	Second order elastic moduli	force/area	dyn/square centimeter	5.5
D_{Be}, D_{Ga}	Be, Ga diffusivity	diffusivity	square centimeter/ second	5.5
Be_i^+	Beryllium interstitial symbol	none	none	5.5
Be_{Ga}^-	Beryllium-on-gallium site symbol	none	none	5.5
Ga_i^0	Gallium interstitial symbol	none	none	5.5
V_{Ga}^0	Gallium vacancy symbol	none	none	5.5
μ_H	Hole mobility	length ² / voltage-time	square centimeter/ volt-second	6.3
t	Time Active layer thickness	time length	second micron	6.3
μ_{iid}	Degenerate ionized impurity mobility	length ² / voltage-time	square centimeter/ volt-second	6.3

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
Q	Hole wave function symmetry factor	none	none	6.3
μ_H	Hall mobility	length ² / voltage-time	sq. centimeter/ volt-second	6.3
ϕ_{Bp}	Metal/p-semiconductor barrier height	energy	electron-volt	6.3
A_f	Contact field emission areal percentage	none	none	6.3
ρ_{cth}	Thermionic emission specific contact resistance	resistance- area	ohm-square centimeter	6.3
ρ_f	Field emission specific contact resistance	resistance- area	ohm-square centimeter	6.3
f_p	Hole emission probability	none	none	6.3
f_q	Ratio of total current to thermionic current	none	none	6.3
v_{th}	Thermal velocity	length/time	centimeter/second	6.3
v_d	Diffusion velocity	length/time	centimeter/second	6.3
p_s	Hole sheet concentration	carriers/area	carriers/ square centimeter	6.3
N_{AS}	Acceptor sheet concentration	atom/area	carriers/ square centimeter	6.3
r	Ratio of heavy hole mass to light hole mass	none	none	6.3
N_I	Ionized impurity density	ions/volume	ions/cubic centimeter	6.3
Z	Impurity ion valence	none	none	6.3
μ_{al}	Alloy scattering mobility	length ² / voltage-time	square centimeter/ volt-second	6.3

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
V_c	Primitive cell volume	volume	cubic centimeter	6.3
μ_{po}	Polar optical phonon scattering mobility	length ² / voltage-time	square centimeter/ volt-second	6.3
K	Light hole mobility correction factor	none	none	6.3
T_{PO}	Polar optical phonon Debye temperature	temperature	Kelvin	6.3
$\epsilon_{s\infty}$	Semiconductor high frequency dielectric permittivity	capacitance/ length	farad/ centimeter	6.3
μ_{dp}	Deformation potential scattering mobility	length ² / voltage-time	square centimeter/ volt-second	6.3
E_{ac}	Phenomenological valence band deformation potential	Energy	electron-volt	6.3
E_{eff}	Effective valence band deformation potential	Energy	electron-volt	6.3
$C_l(x)$	Longitudinal elastic constant	force/area	dyn/square centimeter	6.3
$C_t(x)$	Transverse elastic constant	force/area	dyn/square centimeter	6.3
γ	Ratio of transverse to longitudinal elastic constant	none	none	6.3
L_G	Field effect transistor gate length	length	micrometer	7.5
W_G	Field effect transistor gate width	length	micrometer	7.5
I_{DS}	Drain-source current	current	milliampere	7.5
I_{DSS}	Saturated drain-source current	current	milliampere	7.5
V_{DS}	Drain-source voltage	voltage	volt	7.5

List of Symbols (Cont.)

<u>Symbol</u>	<u>Nomenclature</u>	<u>Physical Quantity</u>	<u>Common Units</u>	<u>Sect. First Listed</u>
V_{GS}	Gate-source voltage	voltage	volt	7.5
g_{me}	External transconductance	conductance/ length	milli-siemens/ millimeter	7.5

Abstract

The p-channel $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ heterostructure insulated-gate field effect transistor (p-HIGFET) is a candidate for complementary integrated circuits due to superior cutoff characteristics and low gate leakage current. Advancement of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET requires improved source/drain design. Five main tasks were accomplished to achieve this goal. First, thermal limits of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET were investigated. Second, the temperature dependence of bandgap and impurity energies were determined for beryllium doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. Third, high acceptor concentrations were obtained on $\text{GaAs}_{1-x}\text{Sb}_x$ using beryllium ion implantation. Fourth, Au/Zn/Au and Ti/Pt/Au were compared as ohmic contact metallizations to these highly doped layers. Finally, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFETs were fabricated and characterized using Ti/Pt/Au metallization and Be implantation. An array of characterization methods were employed to thoroughly characterize materials and devices including: transmission line measurements (TLM), electrochemical profiling, photoluminescence (PL), atomic force microscopy (AFM), secondary ion mass spectroscopy (SIMS), Auger electron spectroscopy (AES), X-ray diffraction (XRD), cross-sectional transmission electron microscopy (XTEM), selected area diffraction (SAD) and energy dispersive X-ray analysis (EDX). This introspective materials examination and engineering approach yielded an ion implantation and ohmic contact scheme which improved the electrical performance and thermal stability of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET.

This dissertation is dedicated to our Lord, Jesus Christ

"I say to you: Ask and it will be given to you; seek and you will find; knock and the door will be opened to you. For everyone who asks receives; he who seeks finds; and to him who knocks, the door will be opened."

- Jesus Christ (Luke 11:9,10)

OHMIC CONTACT TO ION IMPLANTED GALLIUM ARSENIDE ANTIMONIDE FOR
APPLICATION TO INDIUM ALUMINUM ARSENIDE/GALLIUM ARSENIDE
ANTIMONIDE HETEROSTRUCTURE INSULATED-GATE FIELD EFFECT
TRANSISTORS

I. Introduction

The heterostructure insulated-gate field effect transistor (HIGFET) is a promising device for microwave and digital IC applications [1]-[5]. Simultaneous fabrication of n- and p-channel transistors from the same epitaxial layers permits a complementary device technology. Application of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ heterojunction on InP substrates has demonstrated encouraging results as a p-channel HIGFET [6]. Reliable, low resistance source and drain ohmic contacts are needed to ensure HIGFET viability during fabrication and operation, and for uniform scaling of device geometries. The study of ion implantation parameters and ohmic contacts for p- $\text{GaAs}_{1-x}\text{Sb}_x$ is necessary if reliable HIGFET devices are to emerge from fabrication and survive deployment in integrated circuits. This dissertation addresses the above needs within the confines of materials and device research on both p- $\text{GaAs}_{1-x}\text{Sb}_x$ epitaxial layers and the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET.

The HIGFET device is currently pursued by only a few research groups. These efforts have focused on heterojunction combinations which are compatible with GaAs substrates. Coincidentally, the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction system has received little attention. Therefore, coupling the HIGFET device with the

In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} heterojunction furnishes a framework for original materials and device research.

The objective of this dissertation research is to obtain a reliable, low resistance, ohmic contact for the In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} HIGFET. This objective is met by accomplishing the following tasks:

- (1) Ascertaining thermal stability limitations on the In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} heterojunction as they apply to epitaxial HIGFET structures.
- (2) Measuring basic material properties of p-type GaAs_{0.51}Sb_{0.49} for theoretical modeling purposes.
- (3) Determining optimum conditions for ion implantation and annealing of p-type dopants in GaAs_{0.51}Sb_{0.49}.
- (4) Comparing Au/Zn/Au and Ti/Pt/Au as candidate source/drain metallizations for a self-aligned gate process.
- (5) Characterizing metal-semiconductor microstructure following fabrication and thermal stressing.

The dissertation is organized in a "stand alone" fashion such that a graduate level researcher may read it's contents without requiring reference to numerous other sources. This dissertation is categorized into three main sections. The first section is an introduction containing Chapters II and III. Principles of ohmic contact theory, design and characterization are presented in Chapter II. Chapter III is an overview of the In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} HIGFET and the issue of providing ohmic contact to this device. The present state of research and development for this device is overviewed and the research of subsequent chapters is proposed. The second section is composed of Chapters IV and V. In these chapters, foundations for an ohmic contact to the

$\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET are experimentally explored. Chapter IV examines the thermal limits of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET epilayers, and the temperature dependent properties of p-type $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. Chapter V exhibits realization of highly-doped p-type $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ using beryllium ion implantation. Therefore, the second section imposes thermal limitations and produces a cap layer for ohmic contact formation to the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET. The third section is composed of Chapters VI and VII. Here, candidate source and drain metallizations are explored. Chapter VI shows $\text{Au}/\text{Zn}/\text{Au}$ is an unsuitable candidate. Chapter VII demonstrates the superiority of $\text{Ti}/\text{Pt}/\text{Au}$ as an ohmic contact to Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$. Chapter VII also demonstrates improved HIGFET performance using $\text{Ti}/\text{Pt}/\text{Au}$. Finally, Chapter VIII reviews the work of previous chapters and proposes additional topics requiring exploration for complementary $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFETs.

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II. Theory, Design, and Testing of Ohmic Contacts for III-V Device Applications

This chapter provides background concepts essential for understanding proper design and testing of ohmic contacts for III-V devices. Section 2.1 relates the physics of the metal-semiconductor junction to ohmic contact formation. Also, physical quantities which affect design are explained. Section 2.2 catalogs the ideal qualities of sound ohmic contact design. This section highlights conflicts which occur in design optimization. Section 2.3 defines terms fundamental to electrical measurement of ohmic contacts. Measurement methods are also presented. Section 2.4 provides a survey of microstructural characterization methods used to determine contact morphology and elemental interactions. This series of topics yields an understanding of principles and procedures used in the experimentation of subsequent chapters.

2.1 Theory: The Metal-Semiconductor Junction and Ohmic Contact Formation

In this section the theory of electron transfer in a metal-semiconductor system is presented in order to theoretically demonstrate the impact of controllable parameters on ohmic contact design, fabrication, and operation. The definitions of an ohmic contact are given, and energy band diagrams of the metal-semiconductor junction are explained. In particular, expressions for the specific contact resistance are determined for three different conduction mechanisms which occur at metal-semiconductor junctions. The specific contact resistance is viewed in terms of the physical parameters which control its magnitude and impact ohmic contact design. Finally, the specific contact resistance is provided for two semiconductor systems pertinent to III-V electronic devices.

Before launching into a theoretical treatment it's important to present the common *definitions of an ohmic contact*:

- (1) A source of carriers with an internal electrical resistance which is negligible with respect to the semiconductor electrical resistance [1].
- (2) A source of carriers with a non-negligible internal resistance, but one which obeys Ohm's law for current densities of interest [1,2].

Quantification of whether the internal resistance is "negligible" is determined by suitability in device applications and the ability to compete with existing ohmic contact designs. Either of the two definitions above may not be singularly suitable under certain conditions. A contact which is ohmic by definition (1) will provide low resistance but may have a nonlinear current-voltage relationship. An electrical contact which obeys definition (2) would be linear but may have a resistance which is so high that sufficient current may not flow in the device for a given operating voltage. Ideally, an electrical contact with the lowest resistance and a linear current-voltage relationship is desired.

Electrical contacts to III-V semiconductor devices are delineated into two types: (1) Schottky (otherwise known as rectifying), or (2) ohmic. The delineation is based upon the predominant mechanisms by which electrons transfer across the metal-semiconductor junction. The ohmic contact has a linear current-voltage characteristic, while the Schottky contact is nonlinear.

The energy band diagram for a metal-semiconductor junction is determined by considering the effects on the individual metal and semiconductor materials as they are brought from isolation into increasingly closer proximity, and finally into direct contact. The energy band diagrams are shown in Figure 2.1. The following assumptions and simplifications are made in this treatment:

- (1) The semiconductor material is uniformly doped with an n-type species.
- (2) The device is one-dimensional.

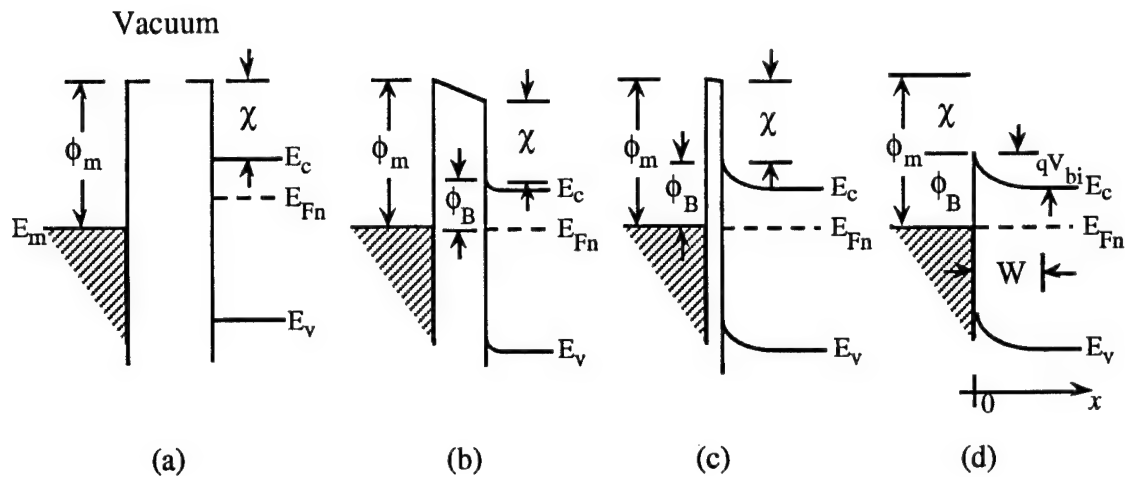


Figure 2.1. Energy band diagrams of an n-type metal-semiconductor junction. (After Sze [2].)

- (3) Charge neutrality holds in both the metal and semiconductor materials.
- (4) The system is in thermal equilibrium with no applied voltage, heat, light or magnetic sources.
- (5) There are no centers for generation or recombination within the semiconductor.

Initially the metal and semiconductor materials are physically and electrically isolated from each other as in Figure 2.1(a). The vacuum level represents the energy level whereby an electron is physically removed from the metal-semiconductor system. The highest occupied energy level in the metal is separated from the vacuum level by an energy amount ϕ_m known as the *work function*, normally given in electron-volts. The energy separation in the semiconductor between the conduction band and the vacuum level is given by the *electron affinity* denoted by χ . In order to maintain charge neutrality, under thermal equilibrium the Fermi levels of the metal, E_m , and semiconductor, E_{Fn} , must come into alignment and remain flat as the separation distance between the metal and semiconductor decreases. Therefore, the conduction, E_c , and valence, E_v , bands within the semiconductor will bend under thermal equilibrium as shown in Figures 2.1(b) - (d). Once

the metal and semiconductor materials are brought into contact, a potential energy barrier, ϕ_B , is formed which prevents electron flow from the metal to the semiconductor. This energy barrier has a characteristic height and width (known as the depletion layer width, W). Barrier height is dependent on the work function and electron affinity. The barrier height is independent of doping density, and hence is independent of the Fermi level position in the semiconductor bandgap. The barrier height energy is derived from Figure 2.1(d):

$$\phi_B = \phi_m - \chi \quad (2.1)$$

A built-in potential, V_{bi} , exists on the semiconductor side of the junction since $\phi_m > \chi$ as illustrated in Fig. 2.1(d). The built-in potential is an energy barrier to electron flow from the semiconductor to the metal due to the difference in E_C between the semiconductor bulk region and the junction. Under forward bias, a positive voltage ($V_A > 0$) is applied to the metal relative to the semiconductor bulk region and the built in potential is reduced by V_A . The electrons are emitted over the barrier from the semiconductor into the metal. Under reverse bias ($V_A < 0$) electrons are emitted over the barrier, ϕ_B , from the metal to the semiconductor. The barrier height, ϕ_B , is kept as small as possible in an ohmic contact, and the doping as high as possible in the semiconductor to minimize W and reduce resistance to carrier flow.

According to Eq. 2.1, the barrier height is made arbitrarily small through the selection of a metal whose work function matches the electron affinity of the semiconductor material. In reality ϕ_B is mostly independent of ϕ_m for III-V semiconductors due to surface states. The surface states are intrinsic to III-V semiconductors and are caused by: (i) the inherent properties of metal-semiconductor interfaces (i.e. metal induced bandgap states), (ii) native defects in III-V materials created by the energy liberated during metal deposition,

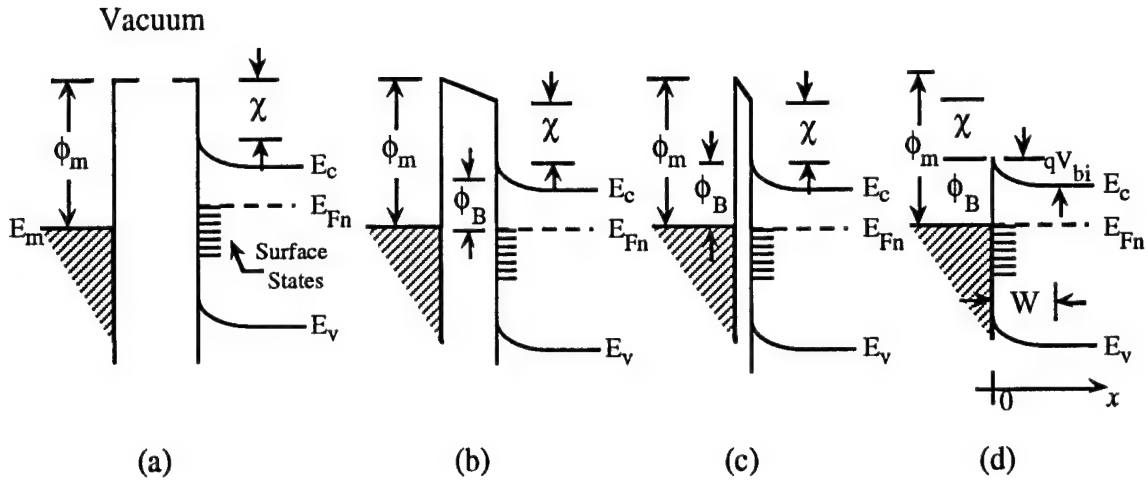


Figure 2.2. Energy band diagrams of an n-type metal-semiconductor junction including the effect of surface states. (After Sze [2].)

(iii) extrinsic III-V semiconductor defects resulting from impurity or metal atom incorporation into the lattice, (iv) dangling bonds at the interface, and (v) work function differences between the metal and microstructural interfacial inclusions of group III or group V elements [3]. These effects "pin" the Fermi level at the surface to the energy level of the highest occupied surface state. The surface states modify the metal-semiconductor energy band diagram as shown in Figures 2.2(a)-(d). Therefore, in a real device, the barrier height is a property of the semiconductor surface and is independent of the metal work function. Thus surface states eliminate the ability of the device engineer to control the barrier height and design an ohmic contact based solely on the metal work function.

The energy barrier width is obtained by assuming an abrupt junction approximation similar to that used in a p^+-n junction analysis [2]. Poisson's equation is

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho}{\epsilon_s} \quad (2.2)$$

(where $\psi(x)$ is the electrostatic potential, ρ is the charge density, and ϵ_s is the dielectric permittivity of the semiconductor), and is solved in the semiconductor subject to the boundary conditions

$$\begin{aligned}\rho &= qN_D & 0 < x < W \\ \rho &= 0 & x > W\end{aligned}\tag{2.3}$$

where N_D is the donor atomic density and W is the depletion layer width. Upon solution of Poisson's equation, the barrier width is written as [4]

$$W = \sqrt{\frac{2\epsilon_s}{qN_D} (V_{bi} - V_A - \frac{kT}{q})}\tag{2.4}$$

where q is the charge on an electron, T is the temperature, and V_{bi} is the built-in electrostatic potential at the metal-semiconductor interface, k is Boltzmann's constant, and V_A is an externally applied voltage. The energy barrier width is therefore a function of the semiconductor material properties (doping, permittivity) and environment (temperature, applied voltage). Thus when designing an electrical contact to a semiconductor device, the designer has the freedom to select the particular semiconductor material and doping level.

The barrier height and width establish a basis for defining which mechanisms govern current flow at the metal-semiconductor interface. The three *dominant conduction mechanisms* are thermionic emission, thermionic-field emission, and field emission [2,5]. Each of the three mechanisms is shown in Figures 2.3(a)-(c). Thermionic emission (TE) is the primary conduction mechanism in lightly doped semiconductors ($N_D < 10^{17} \text{ cm}^{-3}$). In the TE case, the depletion width, W , is relatively wide and conduction electrons must surmount the potential energy barrier. Nonohmic behavior is observed when TE is the dominant mechanism since the junction is highly resistive to current flow until the applied voltage is close to the built in voltage, V_{bi} , (this is a Schottky diode). In the thermionic-

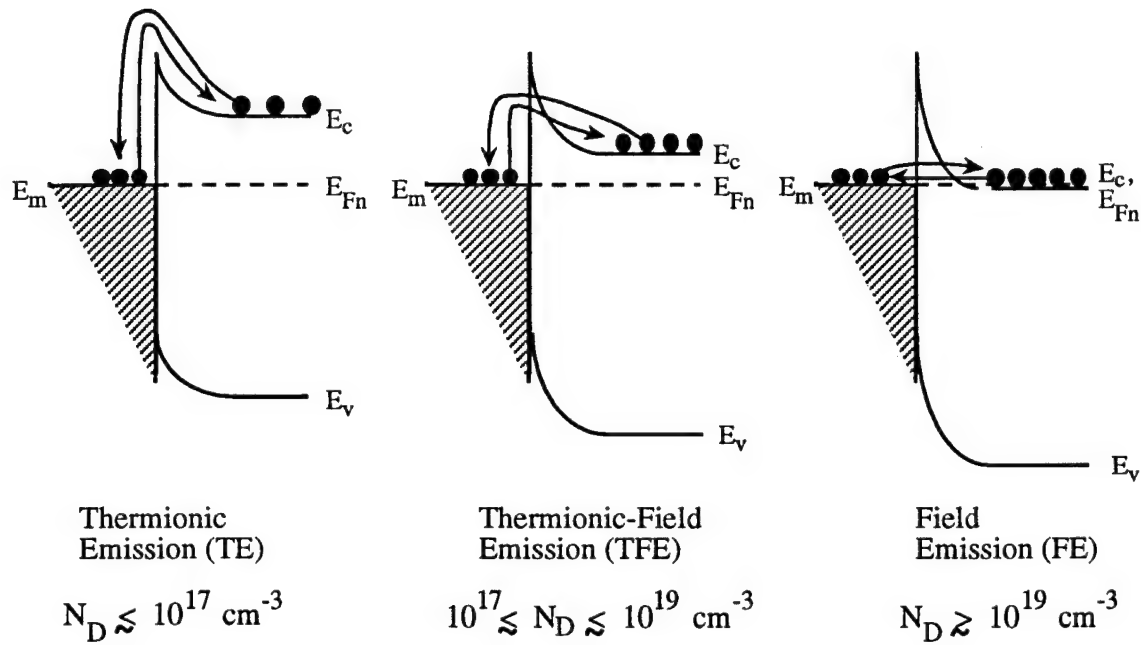


Figure 2.3. Carrier transport mechanisms in an n-type metal-semiconductor junction with increasing doping concentration. (After Schroeder and Meier [6].)

field emission (TFE) regime, thermally excited electrons tunnel through the potential energy barrier at energies above the conduction band but below the top of the potential barrier. TFE applies when the semiconductor is moderately doped ($10^{17} \text{ cm}^{-3} < N_D < 10^{19} \text{ cm}^{-3}$) and the barrier width, W , is reduced relative to the TE case. Field emission (FE) occurs in a heavily doped semiconductor ($N_D > 10^{19} \text{ cm}^{-3}$). The barrier width is narrowest in this case and electrons readily tunnel between the metal and semiconductor.

The basic requirements for an ohmic contact are obtained from the above discussion by applying the definition of an ohmic contact to the metal-semiconductor energy band diagram. In short, a low and narrow barrier is required at the interface. Surface pinning of the Fermi level limits the amount of barrier height reduction obtainable, leaving doping concentration as the remaining adjustable parameter for a given semiconductor. Thus a

highly doped semiconductor layer (capable of providing field emission) produces an ohmic contact with a minimal voltage drop across the metal-semiconductor junction.

An important electrical parameter used to define ohmic contact quality is the *specific contact resistance*:

$$\rho_c = \left(\frac{\partial J}{\partial V_A} \right)_{V_A=0}^{-1} \quad (2.5)$$

where J is the current density. The specific contact resistance is the resistivity of the ohmic contact and has units of $\Omega\text{-cm}^2$. Thus ρ_c is independent of contact area. The specific contact resistance is subsequently expressed for each of the three transport mechanisms. Figure 2.4 illustrates the energy band diagram used in the following discussion.

An expression for ρ_c is determined for the case of field emission by inserting the relationship for $J(V_A)$ into Eq. 2.5. The current density is obtained by considering the quantum mechanical tunneling of an electron from the Fermi level in the metal through the parabolic Schottky barrier to the Fermi level in the semiconductor [4]. This approach is based on a Taylor series expansion of the transmission probability for energies near the Fermi level. The current density in the case of field emission for energies between E_m and E_{Fn} is given by [4]

$$J = \left[\frac{A^*}{(c_1 k)^2} \right] \exp \left[-b_1 \left[\left[\frac{\pi c_1 k T}{\sin(\pi c_1 k T)} \right] \cdot [1 - \exp(-q c_1 V_A)] - q c_1 V_A \exp[-c_1 (E_{Fn} - E_c)] \right] \right] \quad (2.6)$$

where

$$A^* = 4q m^* k^2 \pi / h^3 \quad (\text{the Richardson constant}) \quad (2.7)$$

$$b_1 = (\phi_B - q V_A) / E_{00} \quad (2.8)$$

$$c_1 = \{ \ln[4(\phi_B - q V_A) / E_{Fn}] \} / 2 E_{00} \quad (2.9)$$

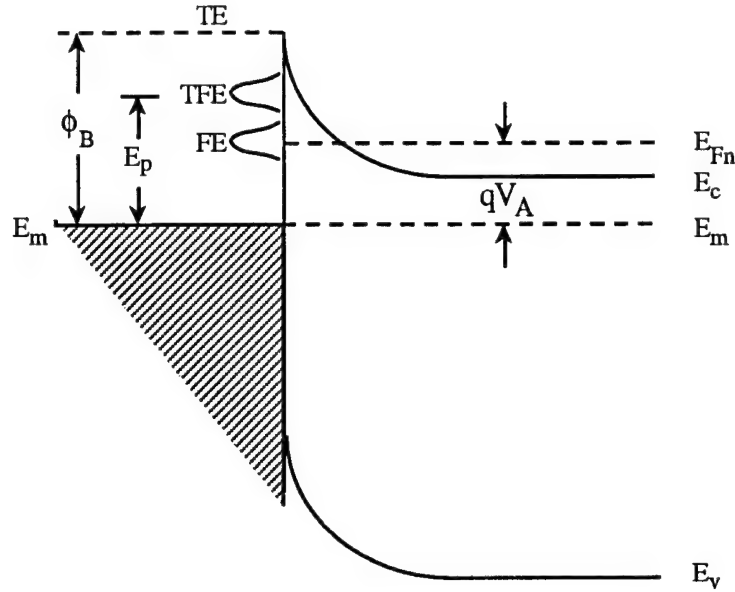


Figure 2.4. Energy band diagram of a degenerately-doped, forward biased, metal-semiconductor junction. The distributions represent the range of energies over which the Taylor series expansion of the transmission probability is made for FE and TFE. (From Padovani and Stratton [7].)

$$E_{00} = \frac{h q}{4\pi} \sqrt{\frac{N_D}{m^* \epsilon_s}} \quad (2.10)$$

Additionally, h is Planck's constant, m^* the electron (or hole) effective mass in the semiconductor, ϵ_s is the semiconductor static dielectric permittivity, and E_{Fn} is the Fermi energy level in the semiconductor. The quantity E_{00} is an energy which characterizes the tunneling process [6]. The expression kT/E_{00} is the ratio of thermionic emission current to tunneling current. For lightly doped semiconductors, $kT/E_{00} \gg 1$ and TE is the dominant conduction mechanism. For heavily doped semiconductors, $kT/E_{00} \ll 1$ and FE is dominant. For TFE, $kT/E_{00} \cong 1$. By placing Eq. 2.6 in Eq. 2.5, a closed form expression for ρ_c is obtained for the FE case [4]:

$$\rho_c = \frac{k}{q A^*} \exp\left(\frac{\phi_B}{E_{00}}\right) \left\{ \frac{\pi T}{\sin(\pi c_1^* k T)} - \frac{\exp[-c_1^*(E_{Fn} - E_c)]}{k c_1^*} \right\}^{-1} \quad (2.11)$$

where $c_1^* = c_1|_{V_A=0}$. The specific contact resistance is thus strongly dependent on ϕ_B and N_D through the exponential term, and weakly dependent on T . In order to emphasize the dependence on N_D , Equation 2.11 is written as

$$\rho_c \propto \exp\left[\frac{4\pi(m^*\epsilon_s)^{1/2}}{qh}\left(\frac{\phi_B}{N_D^{1/2}}\right)\right] \quad (2.12)$$

A similar approach to the FE case is applied to the TFE case in order to obtain an expression for the current density. Here a Taylor series expansion of the transmission probability is performed at the peak energy distribution of the tunneling electrons (E_p , Fig. 2.4) and not at the Fermi level [4]. The resulting expression for the TFE current density is given by [4]

$$J = \frac{A^*T}{2\pi k} \sqrt{\frac{\pi}{f_m}} \left[1 + \text{erf}(E_p \sqrt{f_m})\right] \left[\exp\left(\frac{E_{Fn} - E_c}{kT}\right) - b_m - \left(\frac{E_p - E_c}{kT}\right) \left[1 - \exp\left(\frac{-qV_A}{kT}\right)\right]\right] \quad (2.13)$$

where b_m and f_m are the expansion coefficients of the Taylor series given by

$$b_m = \frac{1}{E_{00}} \left[\sqrt{u(u - E_p)} - \frac{E_{00}E_p}{kT} \right] \quad (2.14)$$

$$f_m = \left\{ 4E_{00}E_p \left[1 - \frac{E_p}{\phi_B} \right]^{1/2} \right\} \quad (2.15)$$

and the parameter u is defined by

$$u = \phi_B - qV_A + E_{Fn} - E_c \quad (2.16)$$

Using Eq. 2.5 an expression for ρ_c is obtained for the TFE case [4]:

$$\rho_c = \frac{(k^2/qA^*) \cosh(E_{00}/kT) [\coth(E_{00}/kT)]^{1/2}}{[(\phi_B + E_{Fn} - E_c) \pi E_0]^{1/2} \exp\left(\frac{E_{Fn} - E_c}{kT} - \frac{E_{Fn} - E_c}{E_0}\right)} \quad (2.17)$$

with

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right) \quad (2.18)$$

Equation 2.17 is dependent on doping concentration through E_{00} and E_0 . Also, the Fermi level position in the semiconductor depends on the doping concentration.

In the case of thermal excitation of conduction electrons to energies above qV_{bi} or ϕ_B at low doping concentrations TE is the dominant transport mechanism. The assumptions made in the development of the current density for the TE case are: (1) the barrier height is much larger than kT , (2) thermal equilibrium is established at the metal-semiconductor interface, and (3) a net current flow does not affect the thermal equilibrium, allowing the superposition of two current fluxes, one from metal to semiconductor and one from semiconductor to metal [2]. The resultant expression for the TE current density is [2,4]

$$J = \left[A^* T^2 \exp\left(\frac{q\phi_B}{kT}\right) \right] \left[\exp\left(\frac{qV_A}{kT}\right) - 1 \right] \quad (2.19)$$

The specific contact resistance for the TE case thus becomes

$$\rho_c = \frac{k}{qA^*T} \exp\left(\frac{\phi_B}{kT}\right) \quad (2.20)$$

Therefore, ρ_c is dependent on barrier height, ϕ_B , and temperature, and is independent of N_D . The TE case presents a maximum value for ρ_c at low doping concentrations.

When Eqs. 2.11, 2.17 and 2.20 are plotted versus doping concentration, each applies only over a particular range of N_D . The three expressions for ρ_c are not limiting cases of each other. For instance, ρ_c for TFE is not obtained by reducing N_D in Eq. 2.11. Figure 2.5 shows a representative view of ρ_c as a function of N_D and displays the region over which a particular transport mechanism dominates. Using Eqs. 2.11, 2.17 and 2.20, theoretical values of ρ_c may be obtained for any III-V semiconductor material. The ρ_c plots permit comparison of candidate semiconductor materials for inclusion as ohmic contact layers in electronic devices. Note that the additional semiconductor material parameters required for obtaining ρ_c are m_e^* , m_h^* , ϵ_s , E_g and n_i (bandgap, E_g , and intrinsic carrier concentration, n_i , are necessary for calculating E_{Fn}). Therefore, in novel material systems being considered for ohmic contact layers these intrinsic parameters must be measured, theoretically calculated or estimated prior to calculating ρ_c .

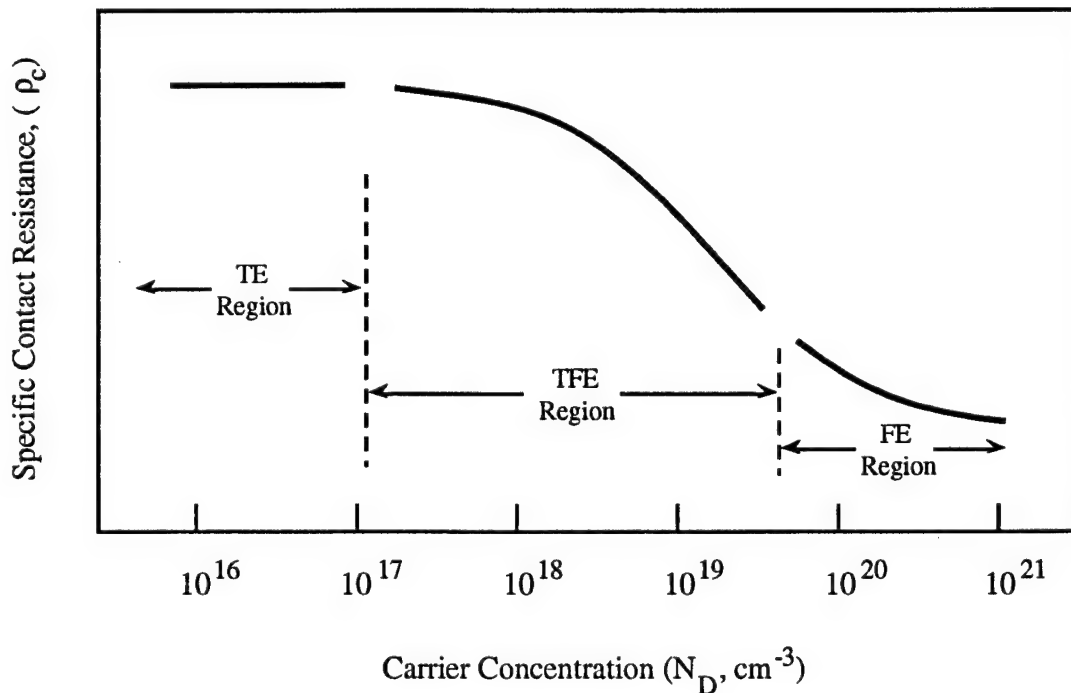


Figure 2.5. Representative graph of specific contact resistance versus carrier concentration at room temperature. Regions over which Eqs. 2.11 (FE), 2.17 (TFE) and 2.20 (TE) apply are indicated.

Image force lowering is an effect which causes additional reduction of the metal-semiconductor barrier height, and hence lowers contact resistance [8]. The electrostatic force between a conduction electron in the semiconductor and the metal surface is the same as the force between a positive charge of $+q$ at the metal surface per electron since the metal is a conductor with an equipotential surface. This electrostatic force drops off rapidly with distance from the metal-semiconductor interface and induces a reduction in the potential energy. Figure 2.6 demonstrates the effect of the image force in reducing the barrier height. The barrier height is reduced by $\Delta\phi_{im}$ and becomes ϕ_{Bn} . Thus in the above equations for ρ_c , ϕ_B is replaced by ϕ_{Bn} when image force lowering is taken into account.

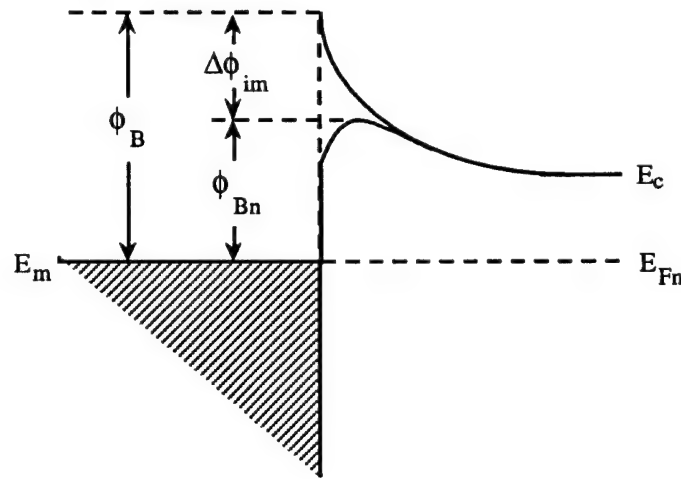


Figure 2.6. Metal-semiconductor energy band diagram illustrating barrier height reduction resulting from image force lowering.

The barrier height lowering caused by the image force is $\Delta\phi_{im}$, given by [6]:

$$\Delta\phi_{im} = \sqrt{\frac{qE_{max}}{4\pi\epsilon_s}} \quad (2.21)$$

where E_{max} is the maximum value of the electric field at the metal-semiconductor interface.

With $V_A = 0$ as in the definition of ρ_c (Eqn. 2.5), E_{max} is expressed as

$$E_{\max} = \left[\frac{2qN_D(V_{bi} - kT/q)}{\epsilon_s} \right]^{1/2} \quad (2.22)$$

Upon substituting Eq. 2.22 into 2.21, a final relationship for $\Delta\phi_{im}$ is obtained:

$$\Delta\phi_{im} = \left[\frac{q^3 N_D (V_{bi} - kT/q)}{8\pi^2 \epsilon_s^3} \right]^{1/4} \quad (2.23)$$

Image force lowering is doping dependent and causes the contact resistance to decrease as the doping is increased, as related in Eq. 2.23. Therefore, in an ohmic contact both the image force lowering and tunneling mechanisms compound at higher doping concentrations ($N_D, N_A > 10^{19} \text{ cm}^{-3}$) and cause reduction of the contact resistance. The image force energy $\Delta\phi_{im}$, is plotted against doping concentration, N_D , for n-type GaAs in Fig. 2.7 for $\phi_B = 0.2, 0.4, 0.6$ and 0.8 eV .^{*} The figure shows that barrier height lowering is greater for larger barrier heights at a given doping concentration. Also, Fig. 2.7 shows the barrier height lowering energy increasing as the doping concentration is increased.

Figures 2.8(a)-(c) and 2.9(a)-(c) present a series of curves of ρ_c versus N_D (or N_A) for semiconductor materials used in III-V electronic device applications. These plots provide ρ_c for a given barrier height, ϕ_B , and doping concentration. The plots were obtained using Eqs. 2.11, 2.17 and 2.20. Each of these plots includes the effect of image force lowering given by Eq. 2.23. The plots are valuable for the following reasons:

- (1) They provide insight into the impact of different material properties on ρ_c .

^{*} Note, specifying ϕ_B simultaneously specifies qV_{bi} because $qV_{bi} = \phi_B - (E_c - E_F)$. The energy separation $(E_c - E_F) = E_g/2 - kT \ln(N_D/n_i)$ [R.F. Pierret, in *Semiconductor Fundamentals*, Volume I, Modular Series on Solid State Devices, R.F. Pierret and G.W. Neudeck eds., Addison-Wesley Publishing Co., Reading, MA, pp. 46-51, 1983].

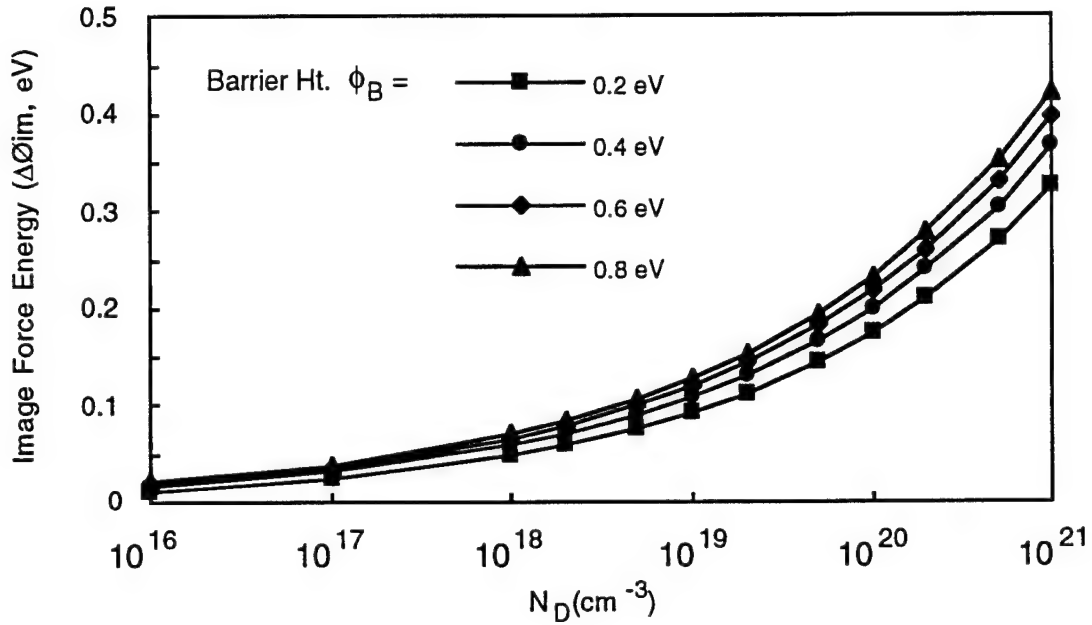


Figure 2.7. Image force lowering energy, $\Delta\phi_{im}$, versus doping concentration, N_D , for n-type GaAs at room temperature. Four barrier height energies are plotted: $\phi_B = 0.2$ eV (square), 0.4 eV (circle), 0.6 eV (diamond) and 0.8 eV (triangle). The plots were obtained using Eq. 2.23.

(2) Comparing expected values of ρ_c for two important classes of III-V semiconductor materials: n-type $\text{In}_x\text{Ga}_{1-x}\text{As}$ and p-type $\text{GaAs}_{1-x}\text{Sb}_x$. The semiconductor materials n- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and p- $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ are chosen since they have application in heterojunction devices, and possess relatively narrow energy gaps when lattice matched to InP substrates.

(3) Ohmic contacts to p-type $\text{GaAs}_{1-x}\text{Sb}_x$ are the primary focus of this dissertation.

Table 2.1 lists the values of E_g , m_e^* , m_{hh}^* (the heavy hole effective mass), n_i and ϵ_s used in the calculations for Figures 2.8 and 2.9, and the corresponding reference.[†]

[†] The symbol, m_0 , in Table 2.1 represents the electron rest mass (9.11×10^{-31} kg).

Table 2.1. Semiconductor Material Properties Used to Calculate Specific Contact Resistance ($T = 300 \text{ K}$).

Semiconductor	$E_g(\text{eV})$	m_e^*/m_0	m_{hh}^*/m_0	$n_i (\text{cm}^{-3})$	ϵ_s
GaAs(n and p)	1.42 ¹	0.068 ¹	0.50 ¹	2.1E06 ¹	13.1 ²
In _{0.53} Ga _{0.47} As(n)	0.75 ¹	0.043 ¹	0.54 ¹	7.5E11 ⁶	14.1 ^{2,5}
InAs(n)	0.36 ¹	0.023 ¹	0.36 ⁴	1.3E15 ¹	15.2 ¹
GaAs _{0.51} Sb _{0.49} (p)	0.78 ¹	0.046 ¹	0.39 ^{2,5}	9.6E04 ⁶	14.3 ^{2,5}
GaSb(p)	0.73 ⁴	0.045 ³	0.28 ¹	5.2E05 ¹	15.7 ¹

¹ "Data in Science and Technology, Semiconductors, Group IV Elements and III-V Compounds", O. Madelung (ed.), Springer-Verlag, NY, 1991.

² S. Adachi, "Materials Parameters of In_{1-x}Ga_xAs_yP_{1-y} and Related Binaries", *J. Appl. Phys.*, vol. 53, pp. 8775-8792, 1982.

³ D.C. Reynolds and T.C. Collins, "Excitons, Their Properties and Uses", Academic Press, NY, p. 271, 1981.

⁴ H.C. Casey and M.B. Panish, "Heterostructure Lasers, Part B", Academic Press, 1978.

⁵ Linear interpolation between endpoint, binary semiconductor values.

⁶ Calculated from the values of E_g , m_e^* and m_{hh}^* .

The first series in Figures 2.8(a) through 2.8(c), demonstrates ρ_c versus N_D for three cases of the n-type In_xGa_{1-x}As system. Figure 2.8(a) illustrates the contact resistance for GaAs for barrier heights of $\phi_B = 0.2, 0.4, 0.6$ and 0.8 eV . Note that ϕ_B cannot exceed the energy bandgap, E_g . The reduction in ρ_c is very apparent as doping density is increased and barrier height, ϕ_B , is decreased. Fermi level pinning (as defined in Section 2.1, Fig. 2.2) in n-type GaAs limits the barrier height to a range $\phi_B = 0.7 - 0.8 \text{ eV}$ [6]. Thus in order to achieve $\rho_c < 10^{-6} \Omega\text{-cm}^2$ (a general ohmic contact design goal for III-V electronic devices), the doping must be very high: $N_D \geq 3 \times 10^{19} \text{ cm}^{-3}$, approximately.

A comparison of the n-GaAs and n-In_{0.53}Ga_{0.47}As plots shows little difference in ρ_c for the same barrier height even though E_g is reduced from 1.42 to 0.75 eV as the In composition is increased. Therefore, reducing E_g for the same value of ϕ_B does not singularly lower ρ_c . The specific contact resistance is lowered when E_g is reduced because Fermi level pinning within the band gap places a maximum limit on ϕ_B . Correspondingly, smaller bandgap materials have a lower ϕ_{Bmax} and thus have a smaller ρ_c for the same N_D . Hence, ohmic contact cap layers in III-V devices consist of highly doped, low bandgap materials to provide a low resistivity transition to the metal contact. However, including these narrow band gap cap layers produces some drawbacks. When capping GaAs with InAs a severe lattice mismatch is encountered - increasing defects and increasing the resistivity of the InAs. Epitaxially grown, highly doped, surface layers produce superior ohmic contact layers. These surface layers are a mixed blessing in III-V FETs since they reduce the Schottky barrier height in gate contacts causing leakage currents, which creates additional processing complexity.

A lower range of ρ_c values for a given N_D is observed in Figure 2.8(c) when comparing InAs to In_{0.53}Ga_{0.47}As and GaAs. Electrical measurements of n-InAs show the Fermi level pinning near the conduction band edge, effectively eliminating any barrier to electron flow [9]. Thus almost any metal provides a good ohmic contact to InAs. Curves for some ϕ_B values at low doping are not complete since the selected barrier height produces an "accumulation" ohmic contact. In the accumulation contact, $\phi_B < E_c - E_{Fn}$; E_c is maximum in the semiconductor bulk and bends downward towards the metal-semiconductor junction. (Accumulation is visualized in Fig. 2.1(d) by supposing E_c is maximum at the right side of the figure and decreases as the junction is approached). An accumulation contact to III-V semiconductors is virtually unattainable due to Fermi level pinning [6]. Curves for some ϕ_B for $N_D > 1 \times 10^{19} \text{ cm}^{-3}$ are not complete since the image force lowering increases until $\Delta\phi_{im} \geq \phi_B$, and no barrier is present.

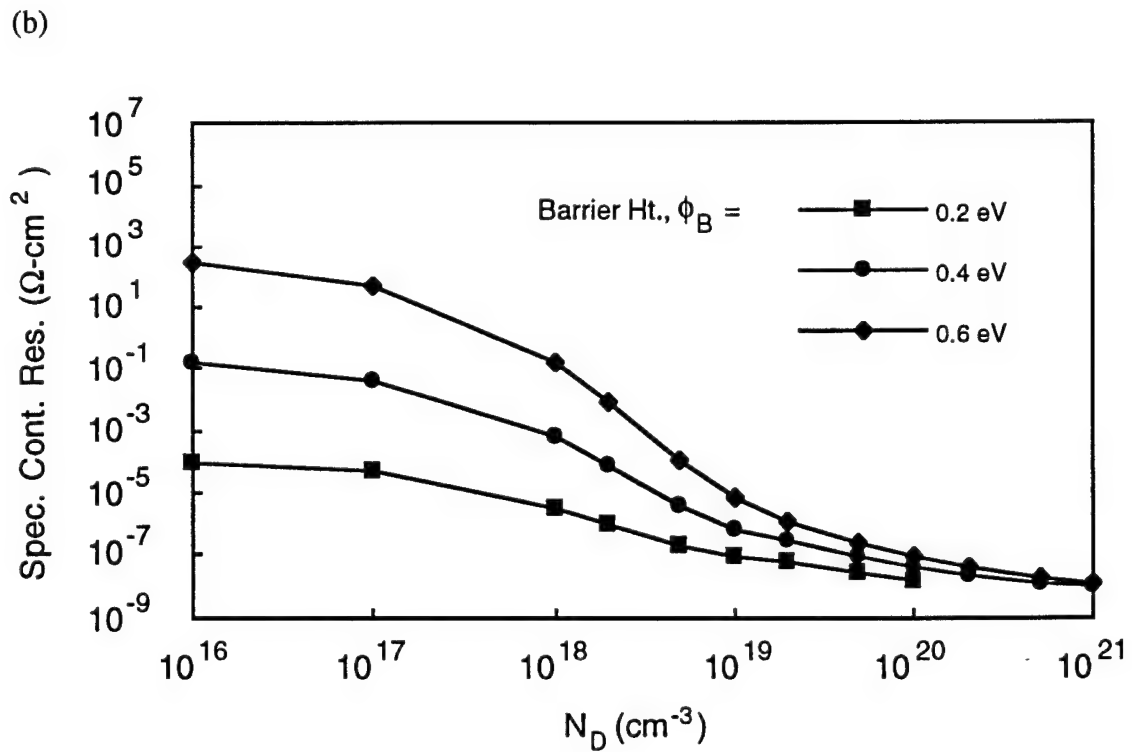
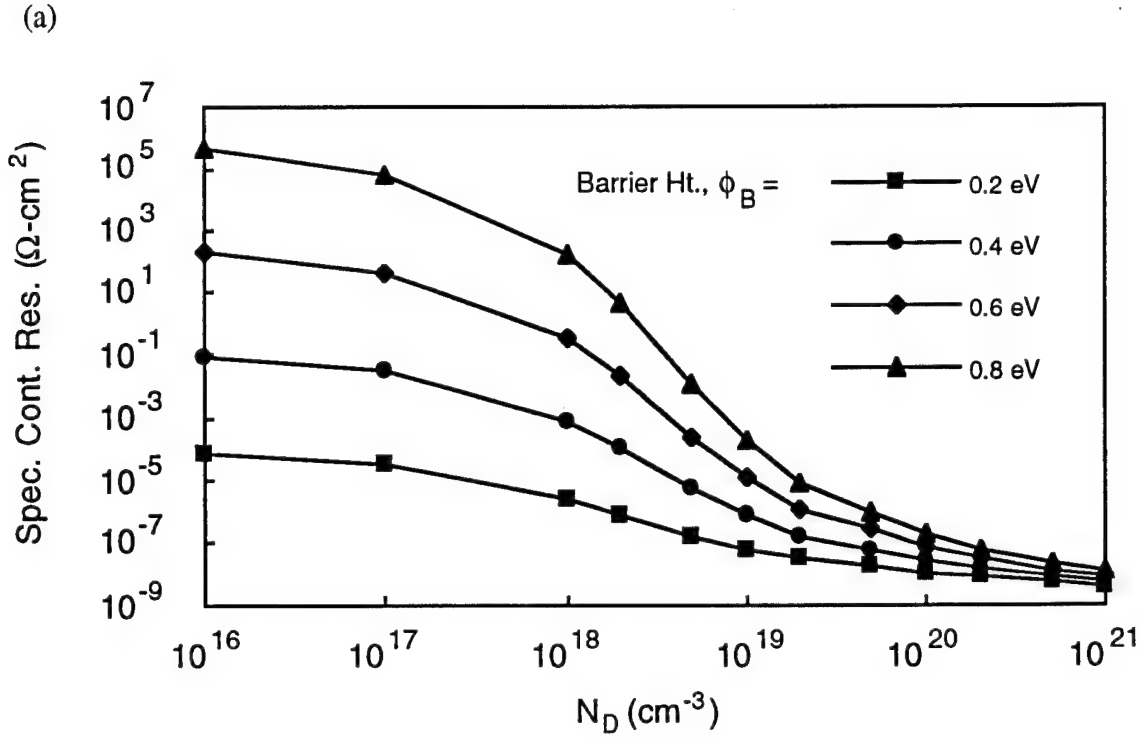


Figure 2.8. Calculated, $T = 300$ K, specific contact resistance, ρ_c , versus doping concentration, N_D , as a function of barrier height for n-type (a) GaAs and (b) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. Image force lowering of the barrier height is included in the calculations.

(c)

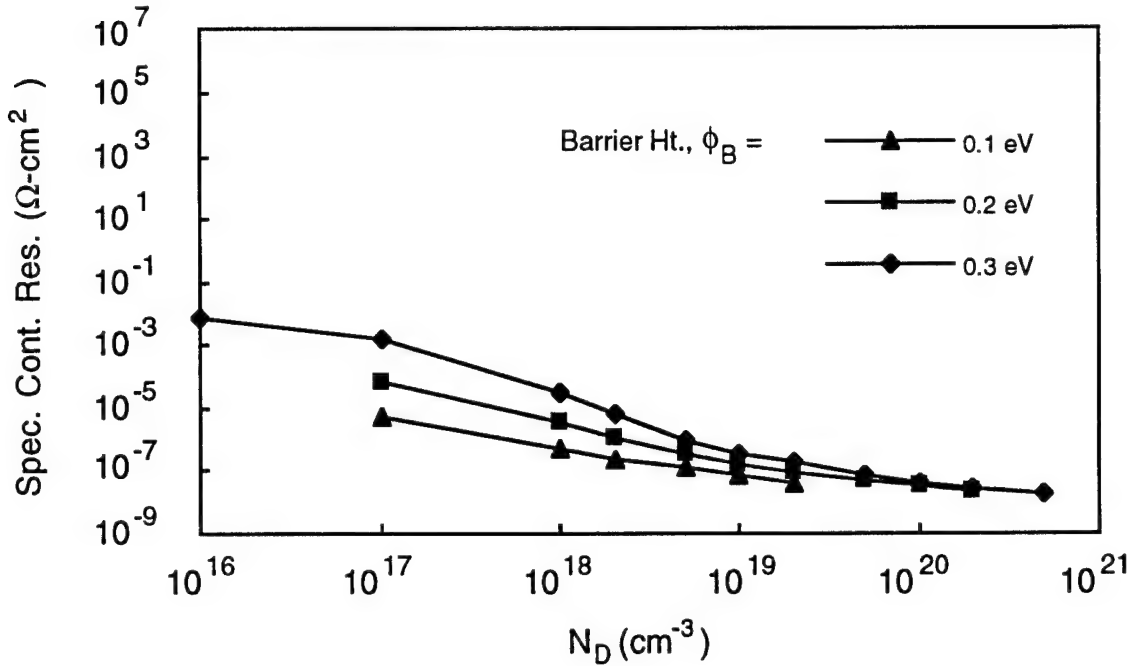


Figure 2.8 (cont.). Calculated, $T = 300$ K, specific contact resistance, ρ_c , versus doping concentration, N_D , as a function of barrier height for (c) n-type InAs. Image force lowering of the barrier height is included in the calculations.

The p-type, $\text{GaAs}_{1-x}\text{Sb}_x$ semiconductor is beginning to receive attention for application in novel III-V electronic devices [10-12]. Figures 2.9(a) through 2.9(c) exhibit the calculated ρ_c versus N_A for three cases of the p-type $\text{GaAs}_{1-x}\text{Sb}_x$ system. An initial comparison of n-GaAs and p-GaAs [Figs. 2.8(a) and 2.9(a)] illustrates the role of effective mass on ρ_c . Since $m_{hh}^* \approx 7m_e^*$, for $N_D = N_A$, ρ_c is lower for n-type GaAs at the same value of ϕ_B . Thus p-type ohmic contacts typically have higher contact resistances than n-type for the same doping concentration. In p-GaAs, the hole barrier height is approximately $\phi_B = 0.5 - 0.6$ eV due to Fermi level pinning [6]. Therefore, the acceptor concentration in p-type GaAs must be in the high 10^{19} cm^{-3} range to obtain $\rho_c < 10^{-6} \Omega\text{-cm}^2$. Doping densities of this magnitude are difficult to achieve in p-GaAs using molecular beam epitaxy (MBE) or ion implantation. However, carbon doped GaAs grown by metal

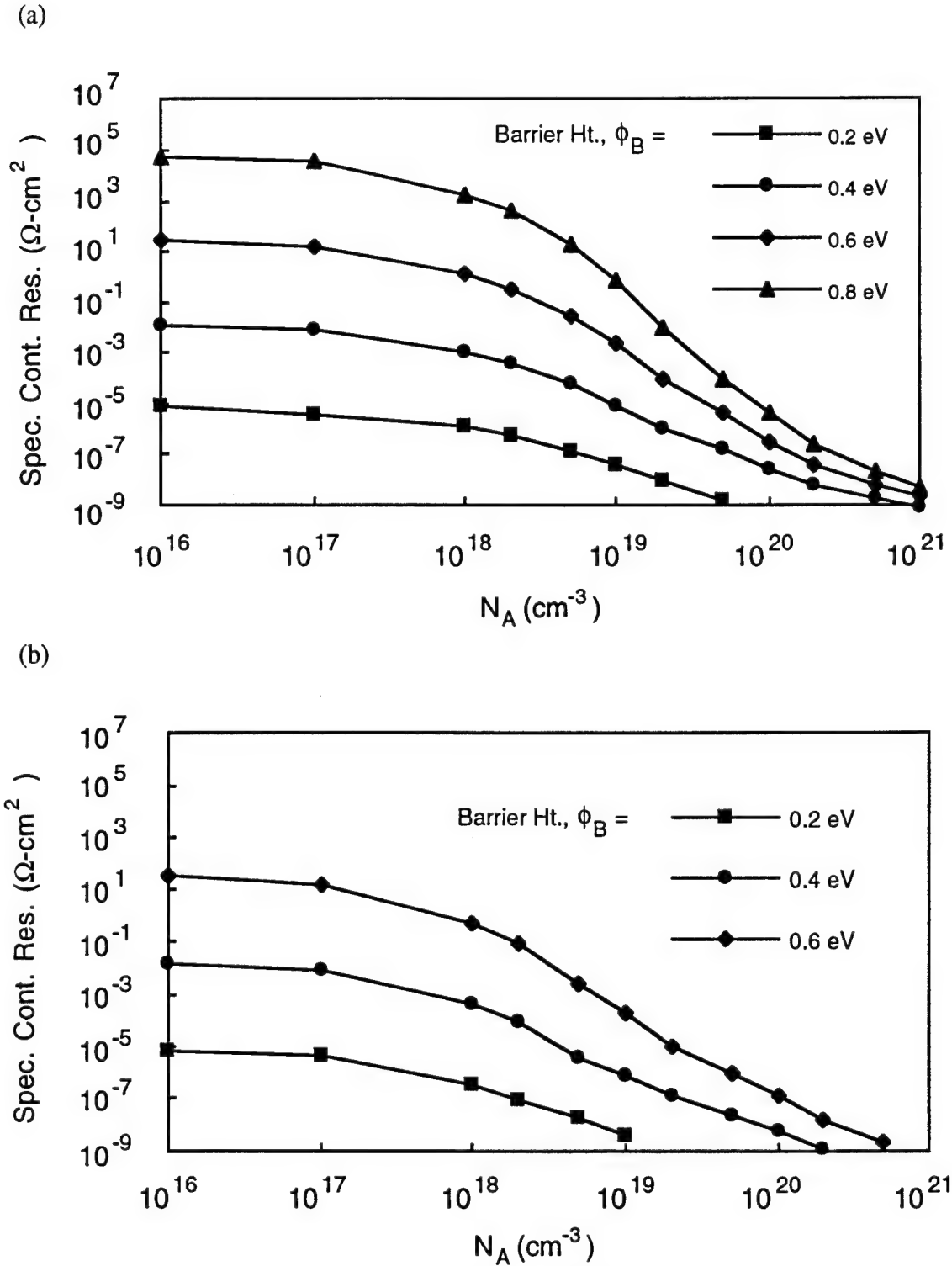


Figure 2.9. Calculated, $T = 300$ K, specific contact resistance, ρ_c , versus doping concentration, N_A , as a function of barrier height for p-type (a) GaAs and (b) $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. Image force lowering of the barrier height is included in the calculations.

(c)

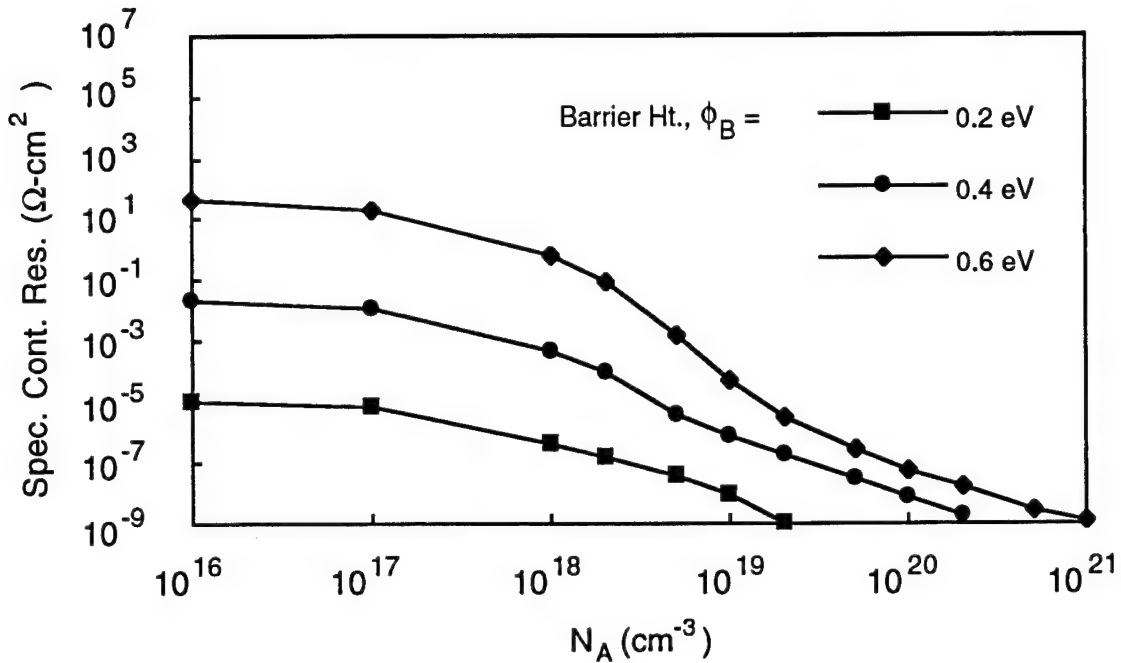


Figure 2.9 (cont.). Calculated, $T = 300$ K, specific contact resistance, ρ_c , versus doping concentration, N_A , as a function of barrier height for p-type (c) GaSb. Image force lowering of the barrier height is included in the calculations.

organic chemical vapor deposition (MOCVD) can achieve doping densities with $10^{19} \leq N_A \leq 10^{21} \text{ cm}^{-3}$ [13]. A trend similar to the $n\text{-In}_x\text{Ga}_{1-x}\text{As}$ system occurs with $p\text{-GaAs}_{1-x}\text{Sb}_x$. The contact resistance reduces as the Sb alloy composition increases due to: (1) the reduction in the maximum attainable ϕ_B as E_g is decreased and (2) the reduced hole effective mass.

2.2 Design Goals for III-V Ohmic Contacts

The preceding theoretical discussion focused on ohmic contact parameters available to the electronic device designer. The discussion demonstrated that obtaining a low contact resistance is predominantly a function of using a narrow band gap, highly doped semiconductor material. Although this requirement seems simple, additional factors must

be considered in order to achieve the goal of a low resistance, ohmic contact for application to III-V electronic devices. The goals include: a linear I-V relationship with low contact resistance, stability (thermal, electrical and mechanical), and conformability to electronic device processing. Often the goals of low resistance, stability, and process conformability are in competition - each cannot always be accomplished without infringing on the other. Additionally, materials, time, and complexity impact the cost of ohmic contact fabrication. Therefore, a thorough understanding of design factors and design goals must accompany consideration of a metal-semiconductor system for application to a III-V device technology.

The design factors and design goals for a good ohmic contact to III-V compound semiconductors are presented in Table 2.2 [5]. Prior to selecting a candidate metallization scheme each of these items must be considered. Monitoring of these factors must occur during contact fabrication and testing. Since all factors cannot usually be satisfied, key factors must be ascertained and prioritized.

Low specific contact resistance and sheet resistance are the primary electrical design goals for an ohmic contact (sheet resistance definition is provided in Section 2.3). The drive to reduce device dimensions, thus increasing operating speed, produces the necessity for reducing the specific contact resistance to $\rho_c < 10^{-6} \Omega\text{-cm}^2$. Reduced electrical resistance is necessary for minimizing power dissipation and device self heating, and reducing carrier transport times in the device by reducing RC charging times.

Process conformability places additional requirements on ohmic contact design and fabrication. Above all, an ohmic contact should not place additional constraints on the ability to exploit III-V materials for particular applications. The number of photolithographic and metal deposition steps should be kept at a minimum during device fabrication. When a complex metallization scheme is used, multiple metal depositions, additional photolithographic steps, and two or more metal deposition systems may be required.

An example of competition between process conformability and device application exists in tungsten-based ohmic contacts to $\text{In}_x\text{Ga}_{1-x}\text{As}$. Tungsten is a preferred metallization in III-V metal-semiconductor contacts due to its high melting temperature and low reactivity. Ohmic contacts employing a tungsten (W) refractory layer are deposited by sputtering. Following sputtering the W layer is patterned and etched to the desired geometry. However, additional metal layers (usually of Au or Al) are required for interconnection and are deposited using evaporation. Thus sputtering, evaporation and etching systems are used in order to make a high temperature, ohmic contact using W. Therefore, the design goal of thermal stability imposes additional process steps (metallization and etching) and requires two types of metal deposition systems - adding cost and complexity.

Additional factors influencing process conformability are ohmic contact formation, reproducibility and yield, and morphology. The highly doped, narrow band gap layers desired for ohmic contacts are obtained through: (i) epitaxially grown semiconductor surface layers, (ii) ion implantation of dopant species and/or (iii) metal contact alloying. Consequently, when one of these three methods for forming an ohmic contact layer is chosen, other aspects of device fabrication may become more complex. Reproducibility and yield are ultimately production level concerns since contact fabrication is done on a large scale using photolithographic, deposition and alloying systems dedicated to a single device technology. The lowest mean ρ_c over the highest percentage of contacts with a minimum statistical variance is sought. Careful consideration is given to new ohmic contact systems before incorporation in integrated circuit manufacturing. Ohmic contact morphology impacts process conformability in terms of reducing device dimensions and photolithographic patterning. Smooth surface morphology is necessary for good electrical and mechanical contact to interconnect metallization and bonding wires. Well defined edge

Table 2.2 Factors and Corresponding Goals for III-V Ohmic Contact Design

Design Factors	Design Goals
<u>Electrical Factors</u> Specific Contact Resistance Sheet Resistance	Low ($< 10^{-6} \Omega\text{-cm}^2$) Low ($< \text{a few } \Omega/\text{Sq}$)
<u>Process Conformability</u> Lithography Ease of Fabrication Reproducibility & Yield Morphology	Fewest layers, moderate thicknesses, round edges Simple deposition, mass producible, wide process window High (values determined by process) Smooth (uniformity determined by process)
<u>Stability Factors</u> <u>Electrical</u> Electromigration <u>Thermal</u> Expansion Coefficient Metal/Semiconductor Diffusivity Process Temperatures Reliability <u>Mechanical</u> Corrosion/Oxidation Stress to Semiconductor Adhesion to Semicond.	None Close to that of the III-V semiconductor material Low (unless appropriate diffusion barriers are used) Withstand 400 °C for packaging and alloying Withstand implant activation temperatures No change in p_c at 250 °C for at least 100 hrs Good - minimal oxidation None Good

morphology is essential for subsequent mask alignments and for preventing electrical shorts between lines separated by small distances.

A good ohmic contact must also possess electrical, thermal and mechanical stability during device fabrication and operation. Electrical instability is usually caused by operating

electronic devices at high current densities. In submicrometer devices the current densities throughout the metal film and contact window can be greater than 10^5 A/cm^2 - generating temperatures of 150°C due to self heating [5]. Also, electric fields between electrodes are large due to narrow interelectrode spacing. Electromigration [14,15] causes a continuous impact of electrons on the metal grains of a contact. The metal grains move in the direction of the current flow until there are regions of excess metal and metal void - creating either an open circuit or wire bond lifting. Currently, very few published results concerning electromigration in metal films on III-V semiconductors are available.

Thermal stability is an area of extreme importance in ohmic contact selection for III-V electronic devices. Ohmic contacts must remain thermally stable during both device fabrication and operation. During device processing, temperatures of $800 - 900^\circ\text{C}$ are common for ion implantation anneals. Also, vertical III-V devices such as heterojunction bipolar transistors may require up to three alloys at temperatures near 400°C for the emitter, base and collector ohmic contacts. In addition, considerable interest exists in high temperature (approximately 300°C) operation of GaAs-based microwave circuits [16,17]. Thus thermal stability of ohmic contacts is of paramount concern considering a device may encounter a number of high temperature thermal cycles during fabrication followed by continuous operation in a high temperature environment. The main cause of thermal instability in III-V ohmic contacts is interdiffusion of the metal and semiconductor elements.

Mechanical stability is usually a function of deposition, alloying and operating conditions. Refractory metals such as W oxidize at temperatures above 500°C [18]. Subjecting W layers to high temperature implants or alloys will cause a high electrical resistance layer to form at the surface if there is oxygen in the environment. Corrosion occurs when metallization is destructively attacked by a chemical or electrochemical reaction caused by the environment. Corrosion results from moisture penetrating into the

metallization and forming an electrolyte between metals of differing electronegativity [15]. Corrosion is prevented by choosing metals with similar electronegativities, removing moisture during deposition and following lithography, and placing fabricated circuits in hermetically sealed packages. Oxidation or corrosion further prohibit good contact of interconnect metallization and wire bonds to the ohmic contact metallization. For good adhesion, metal thicknesses must be minimized and thermal expansion coefficients must be matched between the metal and semiconductor in order to reduce residual stress. Poor adhesion causes the contact metal to separate from the semiconductor surface during photoresist removal and wire bonding.

2.3 Electrical Analysis of Ohmic Contacts

Measurement methods exist for the electrical characterization of ohmic contacts. In this section, terms are defined which describe the electrical resistance of the ohmic contact. Also the theory behind the transmission line model (TLM) is presented. The TLM measurement is the primary electrical measurement method to be used in the research phase of this dissertation.

Figure 2.10 demonstrates a simple ohmic contact geometry. Two metal contacts are separated by a distance "L" defined by a rectangular piece of semiconductor material. The area of the metal-semiconductor interfacial surface is "A". Thus the total, electrical resistance (R_T) of the two metal contacts and the semiconductor piece is

$$R_T = 2R_c + \rho \frac{L}{A} \quad (2.24)$$

where ρ is the resistivity of the semiconductor material. The quantity R_c is the *contact resistance* of the ohmic contact and has units of ohms (Ω). The fundamental unit of measure for ohmic contact resistivity is the *specific contact resistance*, ρ_c (also known as the specific contact resistivity, contact resistivity, and unfortunately, the contact

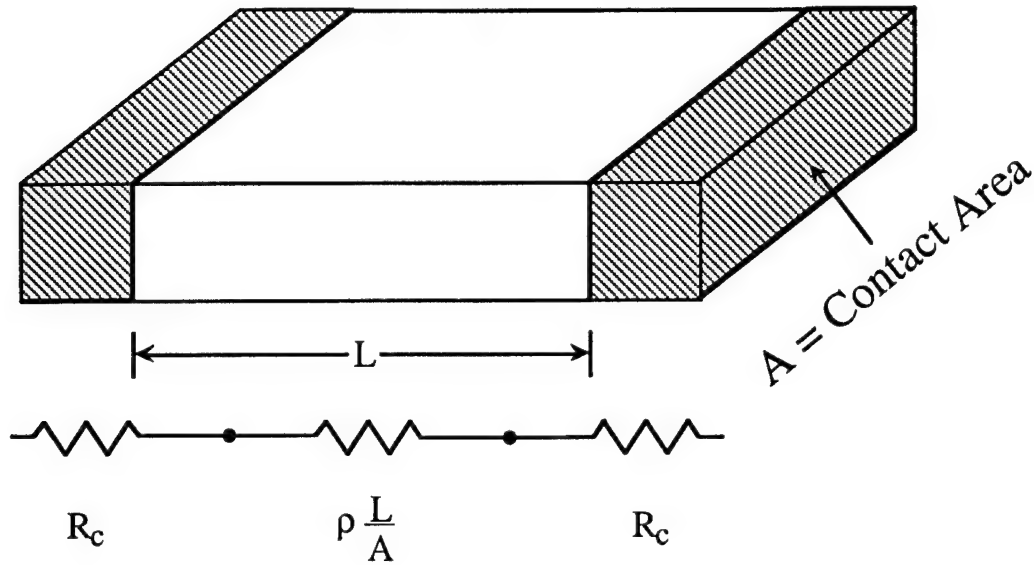


Figure 2.10. Geometry and total resistance of a rectangular ohmic contact. The total resistance of two ohmic contacts is the resistance of the semiconductor plus the two contact resistances.

resistance [1]). A definition for ρ_c was given previously in Eq. 2.5. For the geometry of Fig. 2.10, ρ_c is simply expressed (in units of $\Omega\text{-cm}^2$) by

$$\rho_c = R_c A \quad (2.25)$$

Equation 2.25 defines the resistance of a unit area contact with current flowing perpendicular to the metal-semiconductor interface.

Most contact resistance parameters are measured using planar contacts with rectangular geometries. Fig 2.11 shows the geometries used to describe the coplanar ohmic contacts frequently encountered in lateral FET devices. Current flow is not uniform in the case of coplanar contacts. Current crowding occurs at the edge of the ohmic contact. As device dimensions are scaled down in area by a factor K^2 , R_c does not increase by the same factor but increases somewhere between K and K^2 due to current crowding [19]. Hence, a quantity known as the *transfer length*, L_T , defines the lateral extent of current

flow in or out of the contact until the current magnitude falls to e^{-1} of its value at the edge. The transfer length accounts for current crowding effects in calculations of ρ_c . Most transfer lengths in heavily doped III-V materials are less than one micrometer. Therefore, an ohmic contact with a length of 10 μm or greater is usually considered semi-infinite for modeling purposes [20]. Often in planar contacts the contact resistance is scaled by the width (W) of the ohmic contact. Thus R_c is quoted in units of $\Omega\text{-mm}$. (The name contact resistance is predominantly used when R_c is scaled by W . However, the terms normalized contact resistance, or specific transfer resistance are also used in this case). The fundamental impact of using coplanar contacts is the change in area over which the contact resistance, R_c , is defined. The area is $W \cdot L_T$ for coplanar contacts. Finally, there is an electrical resistance parameter known as the *sheet resistance*, R_{sh1} , which is obtained from

$$R_c = \frac{R_{sh1} L_T}{W} \quad (2.26)$$

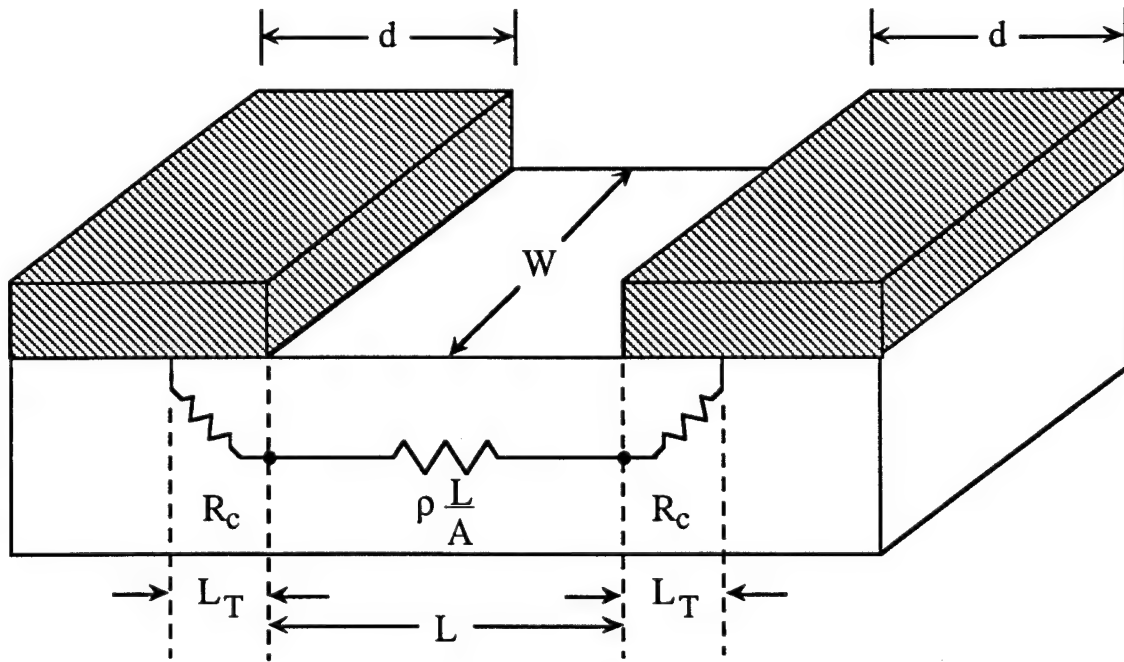


Figure 2.11. Profile of planar ohmic contacts to a semiconductor. The ohmic contact resistance is defined over the transfer length, L_T . In the distance L_T the current reduces to e^{-1} of its value at the contact edge.

with units of Ω/square (Ω/sq). The sheet resistance is the contact resistance when $L_T = W$, as per Eq. 2.26. The sheet resistance underneath the metal is designated R_{sh1} , while the semiconductor sheet resistance between the metal edges is named R_{sh2} .

The most popular method for measuring contact resistance is the transmission line model (abbreviated TLM, also known as the transfer length method and three terminal resistor) developed by Shockley [21]. The equivalent circuit model of a planar ohmic contact is shown in Figure 2.12. The network of resistors represents the distributed electrical resistance to current flow underneath the contact. The TLM model is subject to the following conditions [19]:

- (i) The current lines are normal to the metal-semiconductor interface.
- (ii) The thicknesses of the metal and diffusion layers are ignored.
- (iii) The current-voltage characteristic of the contact is linear.

The horizontal resistors have the resistance (per unit length) of the electrically conductive semiconductor layer given by

$$R' = \frac{R_{sh1}}{W} \quad (2.27)$$

The vertical resistors represent the conductance (per unit length) encountered in the metal-semiconductor interface region with conductance

$$G' = \frac{W}{\rho_c} \quad (2.28)$$

The voltage drop in the semiconductor region is written as

$$dV(x) = -R'I(x)dx \quad (2.29)$$

while from Kirchoff's law the current in the semiconductor at a distance x from the edge of the contact is given by

$$dI(x) = -V(x)G' dx \quad (2.30)$$

Two differential equations are derived from Eqs. 2.29 and 2.30:

$$\frac{d^2V(x)}{dx^2} - \frac{V(x)}{L_T^2} = 0 \quad (2.31a)$$

and

$$\frac{d^2I(x)}{dx^2} - \frac{I(x)}{L_T^2} = 0 \quad (2.31b)$$

where L_T is the transfer length defined as [19]

$$L_T = \frac{1}{\sqrt{R'G'}} = \sqrt{\frac{\rho_c}{R_{sh1}}} \quad (2.32)$$

and R_{sh1} is the sheet resistance of the metal-semiconductor interface. Equations 2.31a and 2.31b are solved by applying the boundary conditions

$$V(0) = V_0, \quad \text{and} \quad I(0) = I_0 \quad (2.33)$$

where I_0 and V_0 are the current and voltage at the contact edge. The solution, subject to the boundary conditions of Eq. 2.33, yields

$$V(x) = V_0 \cosh(x/L_T) - R'L_TI_0 \sinh(x/L_T) \quad (2.34)$$

and

$$I(x) = I_0 \cosh(x/L_T) - (V_0/R'L_T) \sinh(x/L_T) \quad (2.35)$$

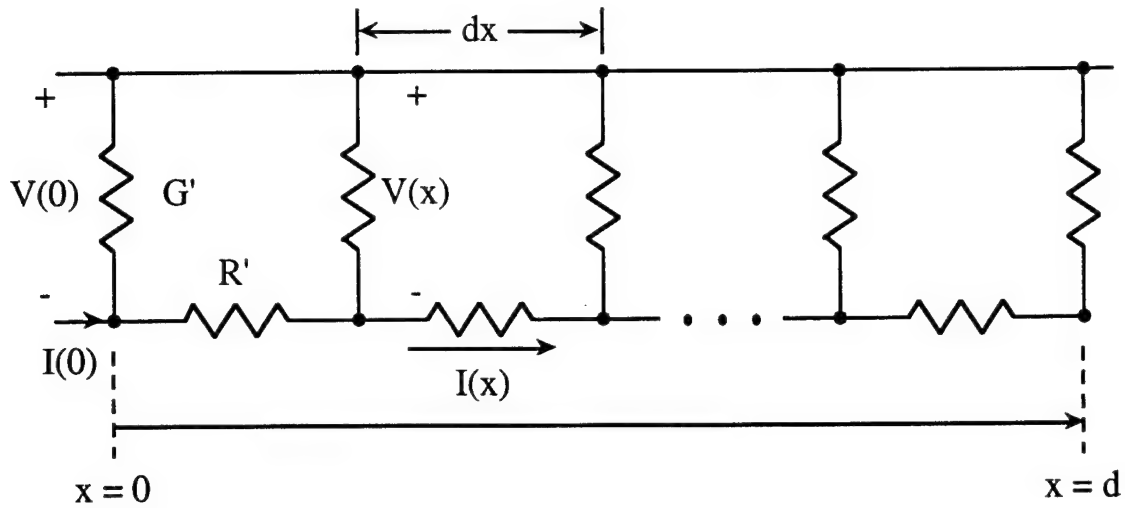


Figure 2.12 Equivalent circuit, transmission line model of the region underneath the metal-semiconductor contact. (After Cohen and Gildenblatt [19]).

Physically, $I(x) = 0$ when $x > d$, therefore $I(d) = 0$. Substituting $I(d) = 0$ into Eq. 2.35 an expression for the contact resistance is derived:

$$R_c = \frac{V_0}{I_0} = \frac{R_{sh} L_T}{W} \coth\left(\frac{d}{L_T}\right) \quad (2.36)$$

This expression for R_c is used with the TLM experimental technique to obtain values for R_c and consequently ρ_c .

A rectangular test pattern used for TLM measurements is shown in Figure 2.13. These "TLM patterns" are fabricated on electrically isolated mesas. The mesas are formed by etch removal of surrounding active layers. Ohmic contact metal is then patterned on the isolated active region and possibly alloyed. There are usually 4 or 5 linearly incremented spacings between the areas containing ohmic contact metal with $L_1 < L_2 < L_3 < L_4 < L_5$. Simply put, ohmic contacts separated by larger spacing have a longer piece of active semiconductor material between them and hence a larger resistance.

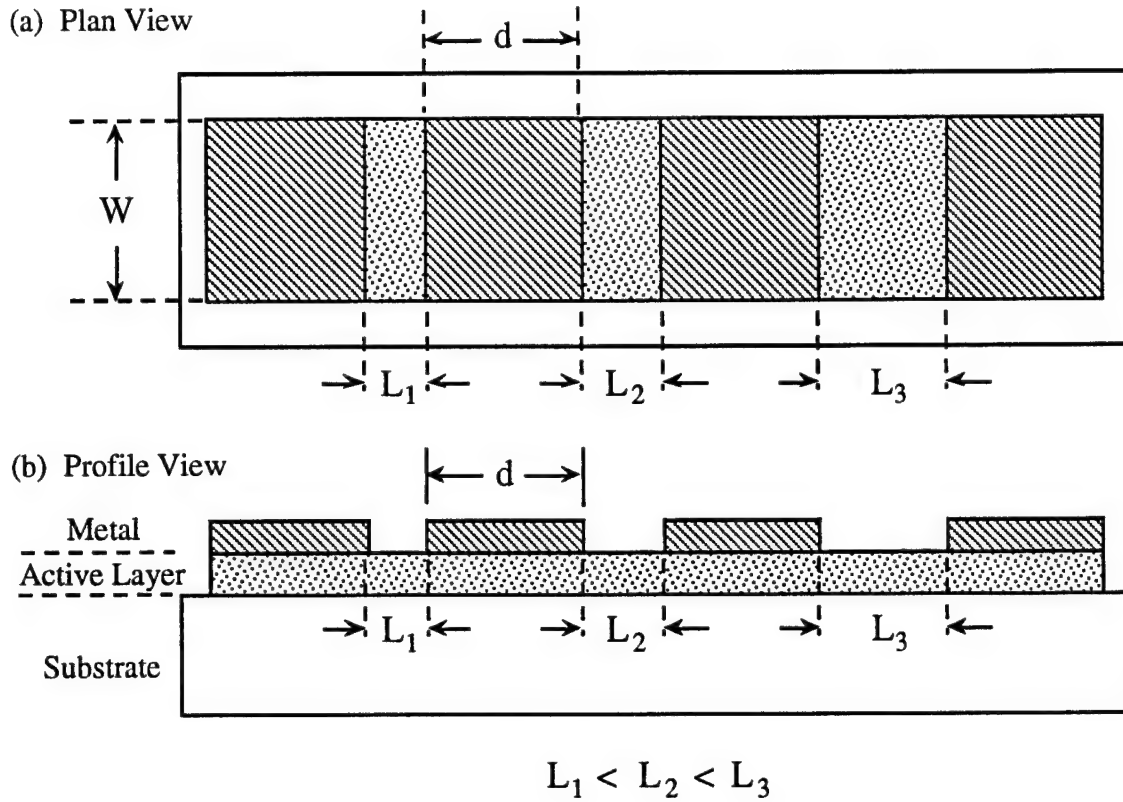


Figure 2.13 Transmission line pattern used to measure contact resistance: (a) plan view and (b) profile view. The spacing between contacts increases from left to right.

A resistance versus length plot is obtained from the TLM pattern (Figure 2.14), where R_T contains the resistance of two of the ohmic contacts and the resistance of the semiconductor material between them, as in Eq. 2.24. Rewriting Eq. 2.24 in combination with Eq. 2.36 yields

$$R_T = 2R_c + \frac{R_{sh2}L}{W} = 2\frac{R_{sh1}L_T}{W} \coth\left(\frac{d}{L_T}\right) + \frac{R_{sh2}L}{W} \quad (2.37)$$

where R_{sh2} is the sheet resistance of the active layer semiconductor material between the ohmic contacts. The goal of the TLM measurement is to obtain a good linear fit to the

experimental data and to extrapolate to the abscissa where $L = 0$. This straight line has a slope of R_{sh2}/W and an abscissa intercept of $2R_c$ according to Eq. 2.37. The $L = 0$ point signifies a zero spacing between the ohmic contact pads. Thus any resistance at $L = 0$ is from the two ohmic contacts only ($2R_c$) and not the active semiconductor material:

$$R_T(L=0) = 2R_c = 2 \frac{R_{sh1}L_T}{W} \coth\left(\frac{d}{L_T}\right) \Rightarrow R_c = \frac{R_{sh1}L_T}{W} \coth\left(\frac{d}{L_T}\right) \quad (2.38)$$

Under the condition that the ohmic metal is electrically long ($d \gg L_T$),

$$R_c = \frac{R_{sh1}L_T}{W} \quad (2.39)$$

and R_c is measured directly from the experiment. Once R_c is known, L_T is determined by setting $R_T = 0$ in Eq. 2.37:

$$L_x = 2 \frac{R_{sh1}}{R_{sh2}} L_T \quad (2.40)$$

The L -axis intercept thus gives $L_T = L_x/2$ assuming the sheet resistances in the bulk semiconductor and under the ohmic contact are equal ($R_{sh1} = R_{sh2}$). The specific contact resistance is then calculated using Eq. 2.32:

$$\rho_c = R_{sh1}L_T^2 \quad (2.41)$$

once L_T is measured.

The accuracy of TLM measurement is limited by (i) assuming equal sheet resistances under and outside of the ohmic contact ($R_{sh1} = R_{sh2}$) and (ii) sources of measurement error. The assumption $R_{sh1} = R_{sh2}$ may not be true, particularly in the case

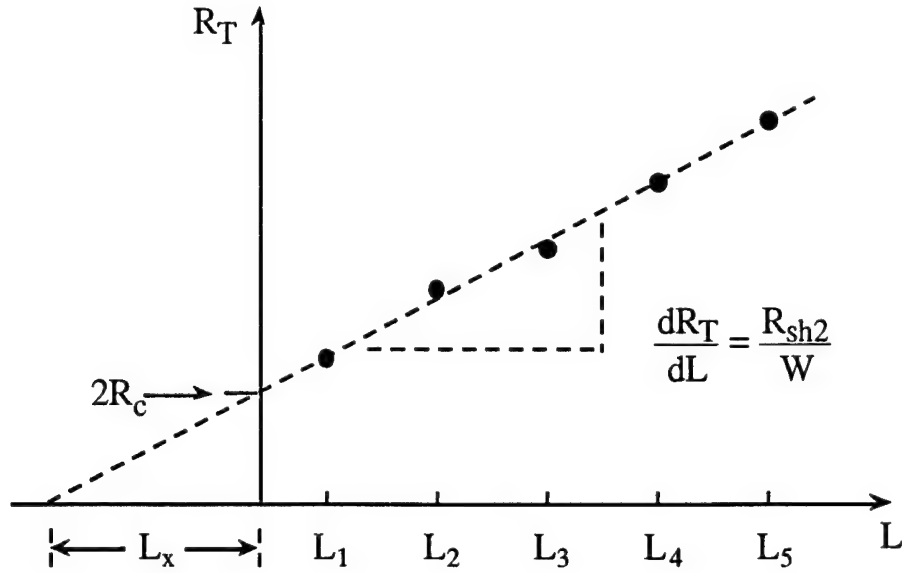


Figure 2.14. Graphical method used in TLM pattern measurements. This method determines contact resistance (R_C), sheet resistance of the semiconductor region between the contacts (R_{sh2}), and transfer length ($L_T = L_x/2$).

of an alloyed ohmic contact where dopant species are thermally diffused into the semiconductor layer beneath the contact. In the case where $R_{sh1} \neq R_{sh2}$ then $L_T \neq L_x/2$, and ρ_c determined by Eqn 2.41 is in error. An additional measurement of the contact *end resistance* (R_E) is made in order to obtain accurate values of L_T and hence ρ_c [19,22]. The experimental configuration used to measure the end resistance is shown in Figure 2.15. In this technique current is passed between two ohmic contacts and the potential between one of these contacts and an outside contact is measured. The value of R_E is then V/I . A combination of Eqs. 2.34, 2.35 and 2.36 allows expression of R_E as [19,23]

$$R_E = \frac{V(d)}{I(0)} = \frac{R_{sh1}L_T}{W} \sinh\left(\frac{d}{L_T}\right) \quad (2.42)$$

Taking the ratio of Eqs. 2.36 and 2.42 yields

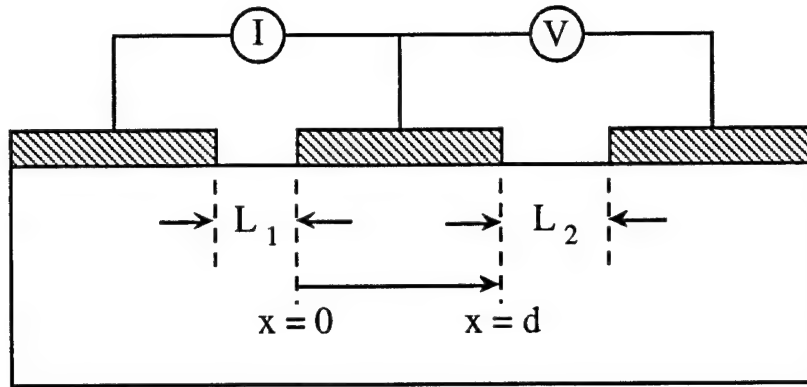


Figure 2.15. Experimental configuration for measuring end resistance, R_E . A current, I , is passed between the left and center contacts. The resultant voltage, V , between the center and right contacts is measured (After Reeves and Harrison [23]).

$$\frac{R_c}{R_E} = \cosh\left(\frac{d}{L_T}\right) \quad (2.43)$$

Thus by taking the end resistance and contact resistance measurements, the transfer length is determined given the ohmic contact length, d . From Eqs. 2.32 and 2.43 a straight forward expression for ρ_c is derived:

$$\rho_c = \frac{W}{d} R_E \frac{\cosh^{-1}(R_c/R_E)}{\sinh[\cosh^{-1}(R_c/R_E)]} \quad (2.44)$$

Determining the specific contact resistance for contacts where $R_{sh1} \neq R_{sh2}$ thus requires measurement of two dimensions (W and d) and two electrical measurements (R_c and R_E).

Care must be taken during TLM measurements to ensure accurate calculation of contact resistance. The basic source of inaccuracy in TLM measurement stems from extrapolating across a wide range of resistance values to a small resistance value (see Fig. 2.14). Therefore, a few precautions are necessary:

- (1) Individual contact spacing should be measured on the TLM patterns using a high power, calibrated, optical microscope or a scanning electron microscope to ensure accurate values of R_T are obtained as a function of L .
- (2) The TLM measurement requires extrapolation from the raw resistance data in order to obtain R_C . Hence, a least-squares, straight line fit to the data must have high correlation for valid measurement of R_C . Correlations of 0.99 or better are acceptable.
- (3) Avoid using high currents (i.e. above 1 mA) in the TLM resistance measurements. High currents exacerbate current crowding effects, induce microstructural contact defects and eventually lead to dielectric breakdown.

2.4 Microstructural Characterization Methods

The previous sections focused on the design of ohmic contacts based upon theory, design factors and goals, and electrical characterization. However, physical factors which form an excellent contact or destroy a contact remain a "black box" unless microstructural characterization methods are employed. This section provides a survey of some of the microstructural characterization methods used in this dissertation research. Each technique for analyzing the microstructure of the metal-semiconductor interface is a science unto itself. Also, more than 20 potential techniques are available for thin film analysis. Therefore, only the pertinent aspects of those techniques applicable to this research effort are highlighted. Each technique is presented in terms of the measurement procedure and benefits/limitations with respect to ohmic contact analysis.

This section focuses on three analytical tools: secondary ion mass spectroscopy (SIMS), Auger electron spectroscopy (AES), and transmission electron microscopy (TEM). Selected area diffraction (SAD) and convergent beam diffraction (CBD) measurements are also taken in the TEM chamber. This battery of techniques provides a

detailed view of metal-semiconductor profiles, elemental interactions, and compound formation. Metal and semiconductor elemental diffusion and intermetallic compound formation may occur during processing, alloying and thermal stressing of ohmic contacts. SIMS and AES are both used for elemental depth profiling and can be used to cross check each other. SIMS yields information on trace element (i.e. dopants) concentration and AES yields concentration percentages. TEM provides information on microstructure geometry by providing a high resolution image of thin film interfaces. SAD and CBD are used to identify elements and compounds based on their crystallographic orientation. There are many excellent references which cover these and other characterization techniques [24-28].

2.4.1 Secondary Ion Mass Spectroscopy (SIMS). The basic measurement process used in SIMS is illustrated in Fig. 2.16(a). An O_2^+ or Ar^+ ion beam is used to sputter through the sample at an energy of 1 to 15 keV. The impact of the incident ions causes the ejection of secondary metal and semiconductor ions from the sample surface. These secondary ions are passed through an energy filter and a mass spectrometer, and are finally detected in a secondary ion detector. The primary ion beam is raster scanned over the sample in a $100 \times 100 \mu m^2$ pattern as in Figure 2.16(b). The secondary ion beam signal is detected from the center of the crater. This scanning process prevents erroneous intermixing of secondary ions from the crater wall with ions from the crater surface. Using this process, SIMS provides the following capabilities:

- (1) Depth profiling to several micrometers with a 10 \AA resolution.
- (2) Detection limits of parts per million (ppm) and parts per billion (ppb).
- (3) Analysis of concentrations of all elements and isotopes.
- (4) Lateral element mapping with a resolution of approximately $1 \mu m$.
- (5) No sample preparation.

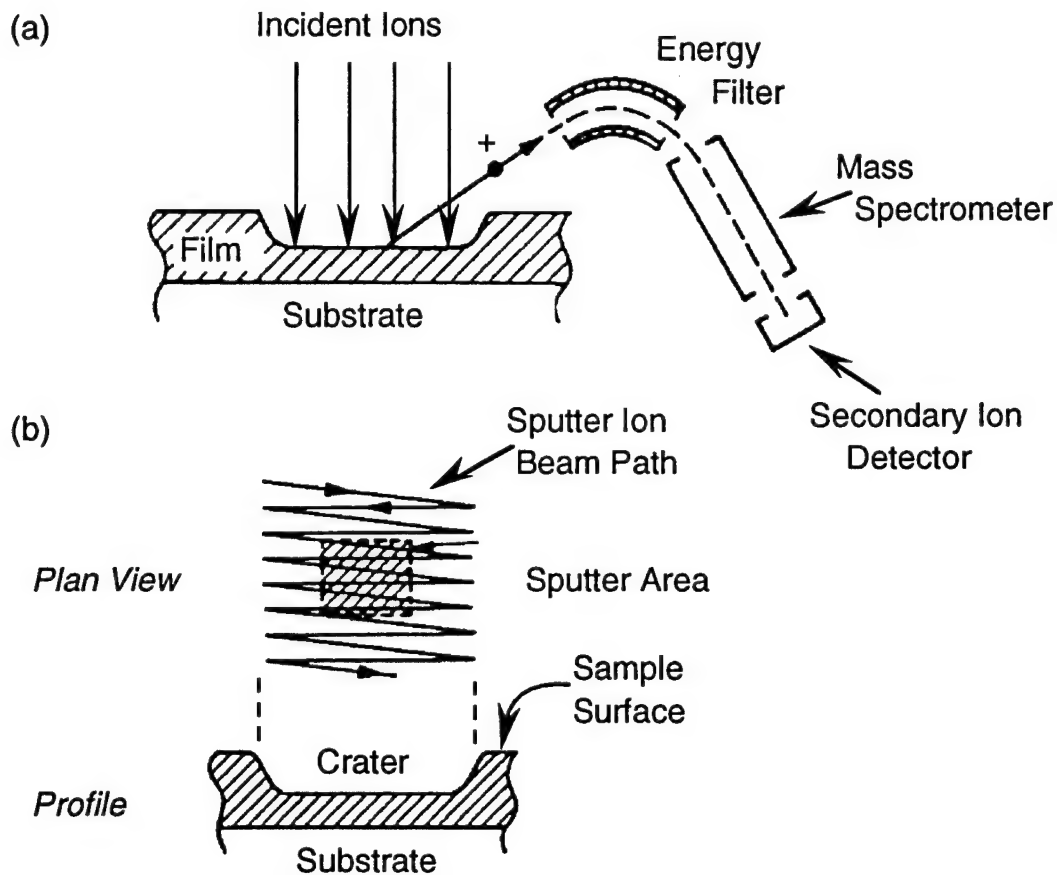


Figure 2.16. (a) Schematic of SIMS measurement system. An incident ion beam ejects surface ions. The ejected ions pass through an electrostatic energy filter and a mass spectrometer and finally into an ion detector. (b) Plan and profile views of the SIMS surface scanning method used to avoid crater edge effects. (From Feldman [24].)

The following limitations exist for SIMS:

- (1) Technique is destructive.
- (2) Knock-in effects due to the primary sputter beam may drive surface level elements into lower layers. Thus a false appearance of metal indiffusion into semiconductor layers may occur when metal film thickness is $\geq 1,000 \text{ \AA}$.
- (3) Detection sensitivities differ depending upon which element requires detection in a host matrix (i.e. detection of Au in a GaAs matrix or Ga in a Au matrix).

Therefore, in a metal-semiconductor system, the most common use of SIMS is the detection and measurement of low concentrations of foreign atoms in a host solid. SIMS thus provides information on metal diffusion into semiconductors (such as Au in a GaAs matrix) or outdiffusion of semiconductor elements into metal layers (such as Ga in a Au matrix).

2.4.2 Auger Electron Spectroscopy (AES). An experimental AES apparatus is shown in Figure 2.17. The sputter ion gun bombards the surface in the same manner as SIMS. A focused electron beam is directed onto the sample surface at the sputter crater. The e-beam produces a cone of Auger electrons, secondary electrons, and X-rays. The emitted Auger electrons pass through a cylindrical mirror velocity analyzer which determines their kinetic energy. The emitted electrons then hit a sensitive electron multiplier which amplifies the signal. This process allows the data acquisition system to measure emitted electron intensity as a function of electron kinetic energy.

The number of emitted Auger electrons is usually small in comparison to the secondary electrons. The Auger electron spectra is superimposed on a large background spectrum. Consequently the first and second derivatives of the detected signal are used to determine the intensity of the Auger electron signal as shown in Figure 2.18. In quantitative analysis the area under the $N(E)$ peaks, the peak-to-peak height (ptph) of the first derivative of $N(E)$ and the base-to-peak height (btph) of the second derivative of $N(E)$ are proportional to the percent concentration of a particular element. The intensities at a single energy are monitored during sputtering to obtain the depth profiling of a particular element.

The Auger process at the atomic level is described by viewing a KL_1L_1 Auger transition in Figure 2.19. The primary electron beam imparts energy to the atom. The atom ejects an electron from the K energy level, thus creating a hole. The ejection of the electron leaves the atom in an excited state. Subsequently, an electron from the higher

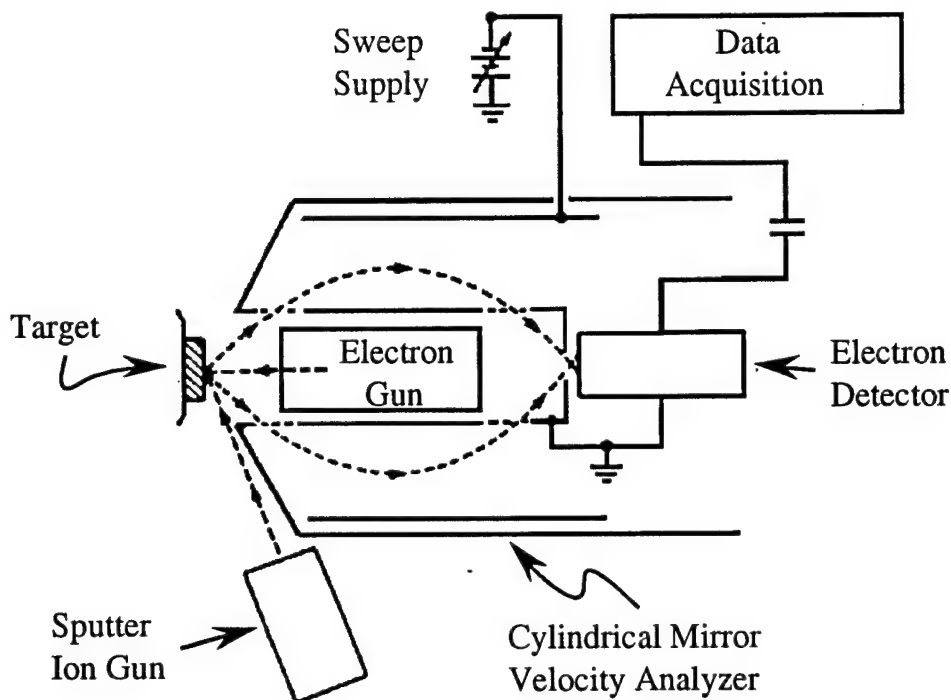


Figure 2.17. Schematic diagram of an AES system. (From Feldman [24]).

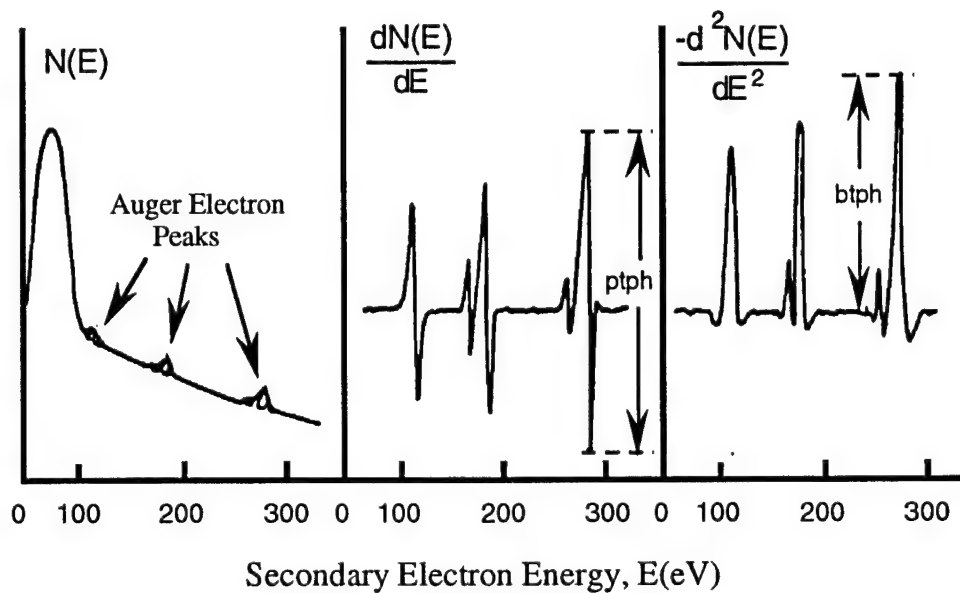


Figure 2.18. Representative AES spectra. The $N(E)$ spectrum includes Auger electron peaks against a broad background of intensity provided by secondary electrons. The zero crossings of the $dN(E)/dE$ spectrum identify the Auger transition energies. The peaks of the second derivative spectrum also identify the Auger transition energies. (From Morgan [28].)

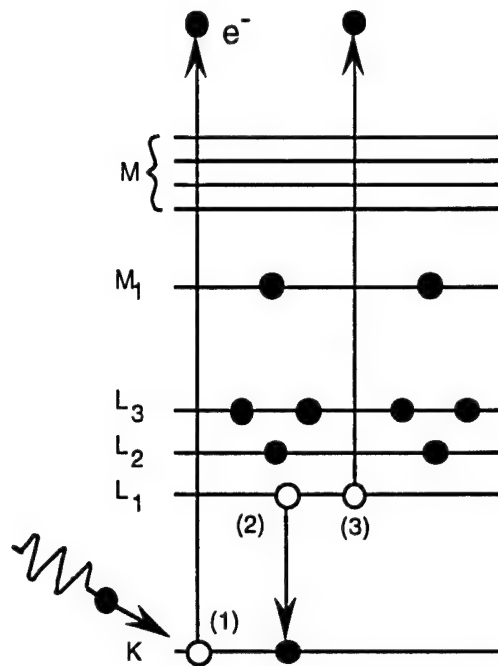


Figure 2.19. Atomic energy level diagram of a KL₁L₁ Auger transition. (1) An incoming electron imparts enough kinetic energy to remove a K-level electron from the atom. (2) An L₁-level electron loses energy and recombines nonradiatively with the K-level hole. (3) The nonradiative recombination energy causes the ejection of a L₁-level electron. (From Feldman [24].)

energy level, L₁, decays into the lower energy hole at the K level. This decay causes the ejection of a L₁ electron into the vacuum. The kinetic energy of the outgoing electron is $E_K - E_{L_1} - E_{L_1}$. This measured energy is thus a function of the atomic energy level structure and provides a signature unique to each element.

AES provides the following capabilities:

- (1) Depth profiling to several micrometers with a 10 Å resolution.
- (2) Analysis of concentrations of all elements except H and He.
- (3) Lateral element mapping with resolution of approximately 0.1 μm.
- (4) No sample preparation.
- (5) Easy detection of low mass impurities such as oxygen or carbon.

The following limitations exist for AES:

- (1) Technique is destructive.
- (2) Knock-in effects are possible due to the primary sputter beam.
- (2) Detection limits are not as good as SIMS - minimum detection limit is 0.1%.

2.4.3 Transmission Electron Microscopy (TEM). In TEM, parallel electron beams pass through a thin specimen, producing an image on a fluorescent screen. A drawing of a TEM system is shown in Figure 2.20. The electron gun consists of a heated tungsten filament, a focusing element and an anode which accelerates the electrons from 100 to 1000 keV. Four or more lenses with axially symmetric magnetic fields are used to control the e-beam. The condenser lens controls the electron illumination intensity and convergence. The objective, intermediate and projector lenses provide magnification of the specimen image. The range of angles of the e-beams emitted from the sample is limited by the objective lens aperture. The objective lens aperture filters out diffracted e-beams when the TEM is in imaging mode. The final image is viewed on a fluorescent screen.

Acceleration of electrons to high energies allows extremely high resolution images. From quantum mechanical considerations, an electron accelerated to 50 keV has a wavelength of 0.055 Å. This wavelength is much shorter than the interatomic distances encountered in metal and semiconductor films and would provide subatomic resolution in the absence of beam divergence. The condenser lens produces a finite divergence of the electron beam. This divergence degrades the quality of the image ultimately limiting resolution to approximately 1 Å.

Cross-sectional TEM (XTEM) is used to obtain images of the metal semiconductor interface. Sample preparation for XTEM analysis is extremely tedious and time consuming. The sample preparation process involves lapping, cleaving, cleaning, epoxying, embedding, polishing, reinforcement, and ion milling. The process can take a

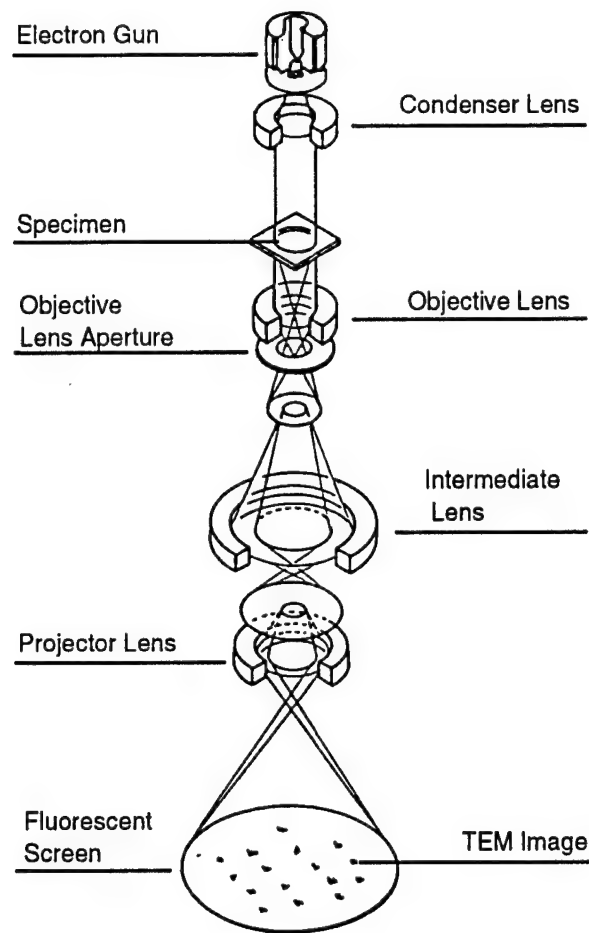


Figure 2.20. Drawing of the internal components of a TEM. Cross-sectional TEM (XTEM), selected area electron diffraction (SAD) and convergent beam diffraction (CBD) are also performed in the TEM chamber. (From Gibson [25].)

week per sample with risk of breakage at each step. A thorough presentation of the preparation process is given by Sheng [26]. The high capital costs of a TEM system (\$800k is common) and long preparation time for XTEM samples drive commercial characterization costs to approximately \$1200/sample versus \$400/sample for SIMS and AES.

Two diffraction measurements are available using the TEM system. *Selected area diffraction* uses the same set of parallel input beams as in the imaging mode (see Fig. 2.21). Parallel electron beams arrive from the condenser lens in both the imaging and SAD modes. The incoming e-beams penetrate the specimen. Some beams pass vertically through the specimen while others are diffracted off of crystallographic planes. All e-beams emitted from the sample are focused on the objective lens aperture. In imaging mode, the e-beams which pass straight through are focused as a bright field on the fluorescent screen. In SAD, the objective lens aperture is widened and a bright field diffraction pattern forms for crystallographic planes which satisfy the Bragg diffraction condition. Thus crystallographic phases can be identified for the entire sample area which is illuminated. The second form of TEM diffraction, *convergent beam diffraction*, focuses the e-beam so that it behaves as a point source above the sample. The incoming beams have an angular spread with respect to the optical axis, allowing diffraction from many more crystallographic planes compared to the SAD mode. CBD uses the diffraction patterns to identify elements and compounds located in particular regions of the metal-semiconductor interface. CBD is performed on specimen areas as small as 100 Å in diameter. Thus specific areas identified by TEM imaging are micro-analyzed for elemental and compound identification. However, analysis of diffraction patterns is more difficult with CBD than with SAD.

TEM, SAD, and CBD provide the following capabilities for metal-semiconductor junction micro-analysis:

- (1) Imaging of thin film profiles with a resolution of 2 Å.
- (2) Macroscopic identification of intermetallic phases using SAD.
- (3) Microscopic identification of microstructural intermetallic phases using CBD with a resolution of 100 Å.

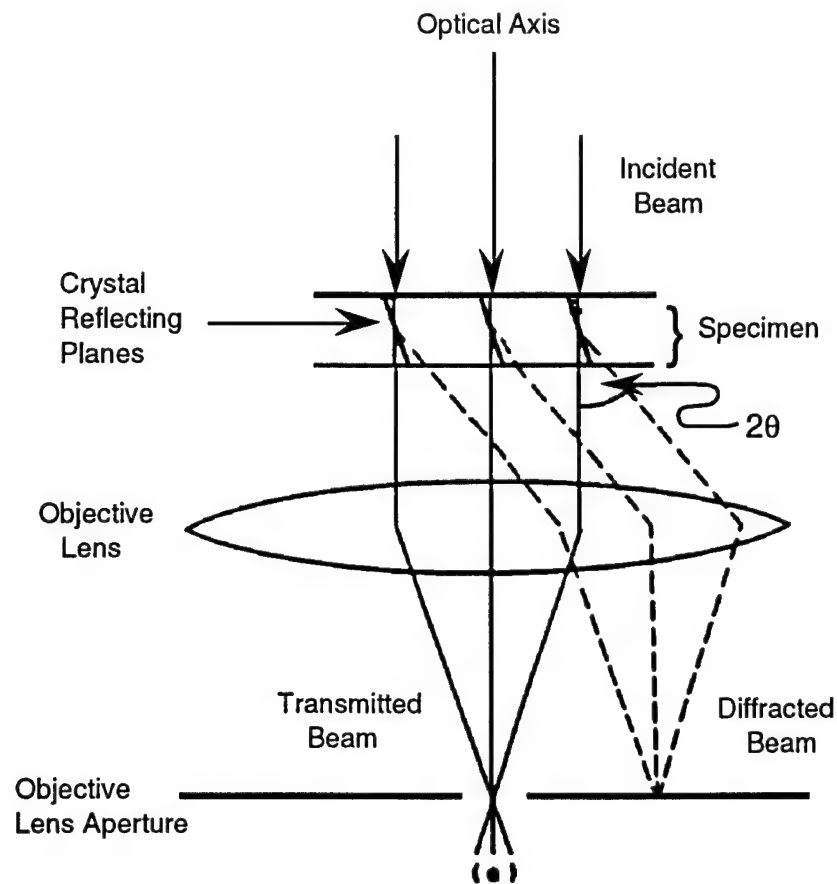


Figure 2.21. Electron beam paths for TEM used in image and SAD modes. The objective lens aperture is widened to allow the diffraction pattern through in SAD mode. (Courtesy of Dr S.D. Walck, Wright laboratory, Materials Directorate, Wright Patterson AFB, OH.)

The following limitations exist for XTEM and SAD:

- (1) Technique is destructive.
- (2) Sample preparation is risky, time consuming and expensive.

Chapter II Summary

This chapter provided essential background concepts for design and testing of ohmic contacts for III-V devices. The physics of the metal-semiconductor junction were

presented in terms of energy band diagrams and transport mechanisms. Equations for specific contact resistance were derived for field emission, thermionic-field emission, and thermionic emission transport mechanisms. Emphasis was placed on the effect of doping concentration, semiconductor band gap, and barrier height on specific contact resistance. The effect of these parameters on ρ_c was demonstrated for n-type $\text{In}_x\text{Ga}_{1-x}\text{As}$ and p-type $\text{GaAs}_{1-x}\text{Sb}_x$. Goals and factors for quality ohmic contact design were catalogued and explained. These explanations included conflicts between design optimization goals. The specific contact resistance (ρ_c), contact resistance (R_c), sheet resistance (R_{sh}) and transfer length (L_T) were defined as they relate to the TLM measurement. The methods, capabilities, and limitations of SIMS, AES and TEM microstructural characterization techniques were surveyed. These topics provide a basis for understanding the material presented in the subsequent chapters of this dissertation.

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III. Ohmic Contacts to InAlAs/GaAsSb Heterostructure Insulated-Gate

Field Effect Transistors

This chapter focuses on the InAlAs/GaAsSb heterostructure insulated-gate field effect transistor (HIGFET) as an electronic device, and fabrication entity. Background and salient features of the HIGFET are presented as well as problematic aspects of producing source and drain ohmic contacts for high performance devices. Section 3.1 views the HIGFET device: its advantages, operating principles, and applications. Singular aspects of the InAlAs/GaAsSb HIGFET are compared to other III-V FET technologies in this section. The dissertation problem statement is substantiated in section 3.2. Here, ion implantation and ohmic contact issues for the self-aligned gate InAlAs/GaAsSb HIGFET are introduced. Section 3.3 gives the objectives of this dissertation research.

3.1 Overview: HIGFET Advantages, Principles and Applications

3.1.1 HIGFET Advantages. In order to operate as a high speed device, the HIGFET takes advantage of a two-dimensional carrier channel and the high carrier mobility offered by III-V materials. The HIGFET is a variation of the high electron mobility transistor (HEMT). It differs from the HEMT by using an undoped gate layer. Some designs additionally exclude extrinsic channel layer doping. The undoped gate layer provides low power dissipation due to low gate leakage currents, and excellent threshold voltage uniformity [1]. Also, undoped channel and gate layers permit fabrication of both n- and p-type HIGFETs using the same epitaxial layers. Thus the HIGFET is attractive as a low power, complementary technology similar to CMOS. A representative, cross-sectional view of self-aligned gate, complementary, InAlAs/GaAsSb HIGFETs is shown in Figure

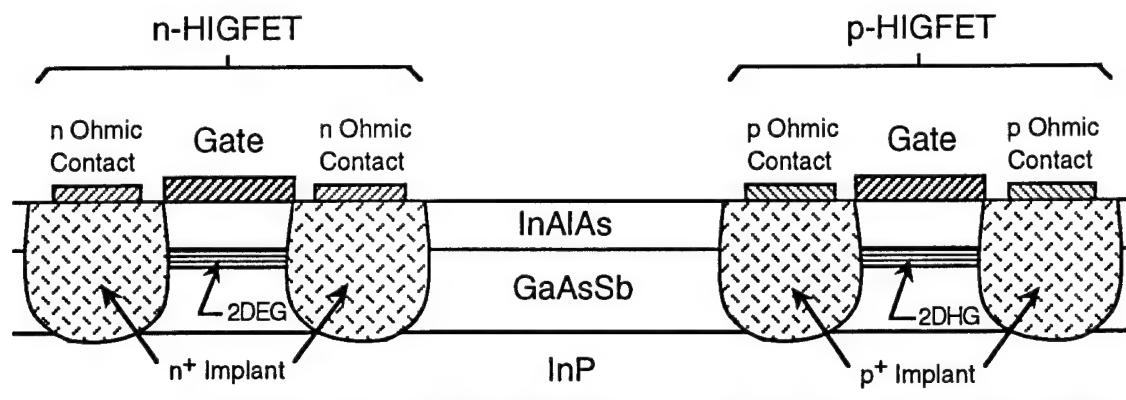


Figure 3.1. Profile view of representative, complementary, InAlAs/GaAsSb HIGFETs.

3.1. The same epitaxial layers are used for both the n- and p-channel devices. The two devices differ only with respect to implant species and ohmic contact metallization. The ion implanted n and p regions provide carriers for the channel. The electrons and holes traverse the channel in a two-dimensional electron/hole gas (2DEG/2DHG). This complementary technology is simple to fabricate and amenable to planarized devices - attributes highly desirable in high density digital technologies.

The InAlAs/GaAsSb HIGFET on InP provides additional advantages over the more conventional $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ system. These advantages are related to the relatively high valence band discontinuity of the heterojunction and the hole mobility of $\text{GaAs}_{1-x}\text{Sb}_x$. The valence band offset for the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction (lattice matched to InP) is $\Delta E_V = 0.64$ eV at 300 K [2,3]. This discontinuity is approximately 4 times larger than the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ system. This higher valence band offset enables superior hole confinement in the $\text{GaAs}_{1-x}\text{Sb}_x$ 2DHG channel. The hole mobility, μ_H , in p- $\text{GaAs}_{1-x}\text{Sb}_x$ is comparable to p-GaAs over a wide range of compositional values (for samples with $x \geq 0.65$ and $N_A - N_D = 2 \times 10^{17} \text{ cm}^{-3}$, $\mu_H \geq 200 \text{ cm}^2/\text{V-s}$ at $T = 300 \text{ K}$) [4]. Strained layer channels should provide additional mobility enhancement through decoupling of the light and heavy hole bands. Initial results on strained layer, p-channel

devices ($x = 0.65$) have demonstrated peak transconductances comparable to other p-channel HFETs, low gate leakage currents, and the highest reported maximum drain current [5]. The advantages of complementary InAlAs/GaAsSb HIGFETs will thus rely heavily on the properties of the p-channel device. This dissertation emphasizes materials research issues which lead to the advancement of a self-aligned gate, p-channel device.

3.1.2 HIGFET Operating Principles. Energy band diagrams for the gate region of the HIGFET device are illustrated in Figure 3.2. The unbiased energy band diagram is shown in Figure 3.2(a) for the undoped, lattice matched $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET. The figure shows a representative HIGFET construction with a 500 Å gate layer and a 200 Å channel layer for growth on an InP substrate. The undoped, wide band gap, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ gate layer provides a large energy barrier to carrier flow from the gate metal to the channel. (Hence, the term "insulated-gate" is used.) The conduction (ΔE_C) and valence band (ΔE_V) offsets are produced by differences in the electron affinity (χ) and bandgap (E_g) respectively between $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ [6]:

$$\Delta E_C = \chi_{\text{GaAsSb}} - \chi_{\text{InAlAs}} \quad (3.1)$$

and

$$\Delta E_V = \Delta E_g - \Delta E_C \quad (3.2)$$

Using the values $\Delta E_V = 0.64$ eV [2], $E_g(\text{In}_{0.52}\text{Al}_{0.48}\text{As}) = 1.45$ eV [7], and $E_g(\text{GaAs}_{0.51}\text{Sb}_{0.49}) = 0.740$ eV [8] at 300 K, gives $\Delta E_C = 0.07$ eV as shown graphically in Fig. 3.2(a). Prior to biasing, the channel layer is essentially devoid of carriers. The Fermi level is near the middle of the energy gap in each of the three semiconductor layers since the layers are undoped. Applying a positive gate bias causes the formation of a 2DEG in the n-channel device (Fig. 3.2(b)). The application of a negative gate bias results in a 2DHG within the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ (Fig. 3.2(c)). Thus the channel carrier type is deter-

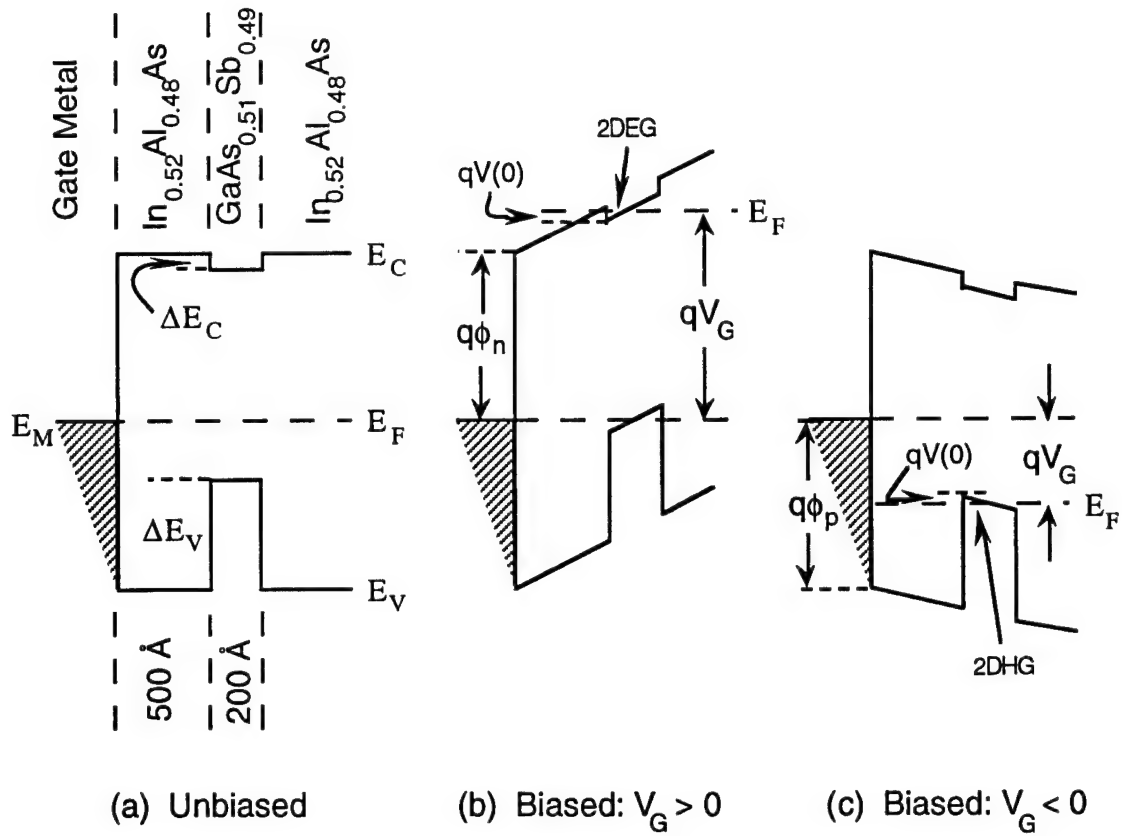


Figure 3.2. Energy band diagram of the gate region cross section for the InAlAs/GaAsSb HIGFET: (a) unbiased, (b) positive gate bias, and (c) negative gate bias. The gate bias produces a 2DEG or 2DHG in the channel. The energy band offsets are ΔE_C and ΔE_V for the conduction and valence bands, respectively. The metal-semiconductor barrier height energies are $q\phi_n$ and $q\phi_p$ for the n- and p-channel devices, respectively. The energy difference between the Fermi energy level and the conduction/valence band at the InAlAs/GaAsSb interface is given by $qV(0)$.

mined by V_G and not by the type of epitaxial dopant in the gate layer as in a HEMT. HIGFETs are enhancement mode devices since the channel is nominally nonconductive with no applied bias.

The threshold voltages for the n- and p-channel devices are extracted from Fig. 3.2. From Fig. 3.2(b), the voltage across the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ insulator layer, $V_{n_{\text{ins}}}$, is expressed as [9]

$$V_{n_{ins}} = V_G - \phi_n + \Delta E_C/q - V(0) \quad (3.3)$$

The gate voltage, $V_G = V_{tn}$, and $V(0) = 0$ at the onset of channel conduction. Therefore, Eqn. 3.3 is written for the threshold voltage as

$$V_{tn} = \phi_n - \Delta E_C/q + V_{n_{ins}} \quad (3.4)$$

Similarly, the threshold voltage for the p-channel, V_{tp} , is obtained from Fig. 3.2(c):

$$V_{tp} = -\phi_p + \Delta E_V/q - V_{p_{ins}} \quad (3.5)$$

where $-V_{p_{ins}}$ is the voltage drop across the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer in the p-channel device. The barrier height for $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ was measured as $q\phi_n = 0.9$ eV [10]. Thus $q\phi_p = E_g - q\phi_n = 0.55$ eV. Combining these values of $q\phi_n$ and $q\phi_p$ with the previously calculated values of $\Delta E_C = 0.07$ eV and $\Delta E_V = 0.64$ eV, gives $V_{tn} \approx 0.83$ V and $V_{tp} \approx 0.09$ V for the InAlAs/GaAsSb HIGFET (assuming $V_{n_{ins}}$ and $V_{p_{ins}}$ are small in relation to their respective barrier heights and energy band offsets). Threshold voltage control and uniformity should be superior in InAlAs/GaAsSb HIGFETs versus HEMTs since the effects of lateral surface dopant inhomogeneity and dopant-induced defect centers are negated by the undoped gate layer [11].

3.1.3 HIGFET R&D Status and Applications. A literature search conducted by the author yielded 44 explicit HIGFET references between the years 1985 and 1995. The two major material systems receiving emphasis for HIGFETs are: (1) $\text{AlGaAs/In}_x\text{Ga}_{1-x}\text{As}$, using either $\text{In}_x\text{Ga}_{1-x}\text{As}$ or GaAs channels (majority contributors: Honeywell and NTT (Japan)), and (2) InAlAs/InGaAs/InP (majority contributors: Honeywell, University of Michigan and AT&T Bell Laboratories). HIGFET research is in a very early stage in

contrast to HEMT and HBT research.* The InAlAs/GaAsSb HIGFET is presently investigated only at Wright Laboratory, Solid State Electronics Directorate by F. Schuermeyer, et. al. The fact that the HIGFET is currently pursued by only a few groups, coupled with the novelty of the InAlAs/GaAsSb system, provides a framework for original dissertation research in III-V materials and devices.

A major emphasis for the HIGFET is rapid deployment from research phase to product development. As of this writing only Honeywell [12] and Motorola [13] are reportedly placing AlGaAs/InGaAs/GaAs HIGFETs in manufacturing processes. A number of IC types were produced from these processes: 4k SRAMs, 16-bit multipliers, adders, and 4-bit A/D converters. The power consumption of a 1 GHz, divide by 256/257, HIGFET prescaler using a 1.1 V supply voltage was only 0.5 mW (10-20 times smaller than GaAs MESFET or Si CMOS) [13]. These initial results are encouraging for ultra-high speed, low power LSI applications.

Future prominence is envisioned for InP-based HIGFET technologies due to the high mobility of $\text{In}_x\text{Ga}_{1-x}\text{As}$ channels [12,14,15]. The InAlAs/InGaAs/InP HIGFET is considered for both digital and microwave applications. Unity current gain frequencies of these devices are as high as $f_t = 87$ GHz [15]. Designs in this material system also use strained channel layers where the In concentration is increased above the lattice matched condition. Strained channel layers modify the energy band structure between the gate and channel layers - allowing larger energy band offsets and increased carrier confinement [14]. An increase in f_t from 22 to 27 GHz was realized using an $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}$ strained channel [14].

The benefits of the InAlAs/GaAsSb/InP HIGFET are not realized unless reliable and efficient, self-aligned gate technologies are developed. The following section

*More than 400 HBT references were obtained by the author through 1992.

highlights important problems in ion implantation and ohmic contact formation which require research in order to advance InAlAs/GaAsSb HIGFET technology.

3.2. Problem Statement: Ion Implantation and Ohmic Contact Issues

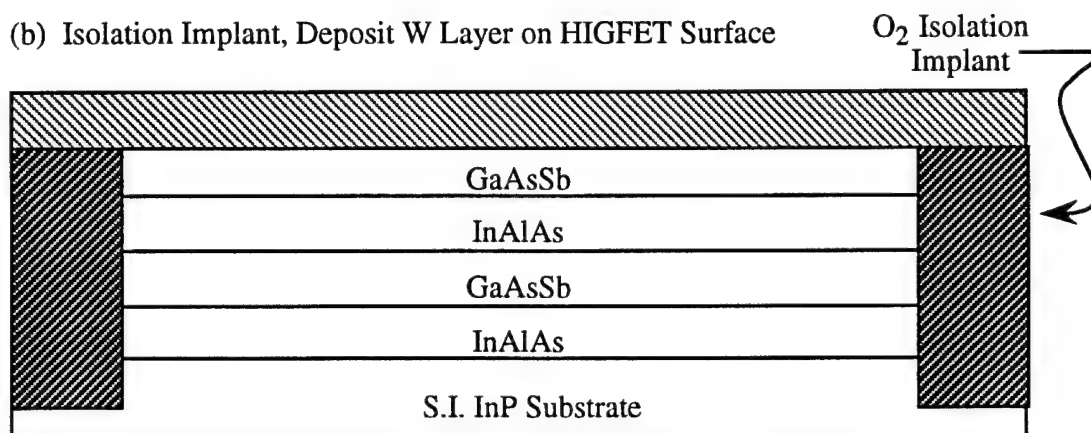
3.2.1 Self-Aligned Gate HIGFET Fabrication Process. The self-aligned gate (SAG) process is presented here to demonstrate critical steps required for HIGFET fabrication. Figures 3.3(a) through 3.3(f) illustrate the SAG process. A cross-sectional view of a representative, as-grown InAlAs/GaAsSb HIGFET structure is shown in Fig. 3.3(a). The HIGFET is grown by molecular beam epitaxy (MBE). Each of the epitaxial layers is lattice matched to the semi-insulating InP substrate. The HIGFET is capped by an undoped, 50 Å, GaAs_{0.51}Sb_{0.49} layer. This cap layer is specified for ohmic contact to the source and drain (S/D) due to the reduction in metal-semiconductor energy barrier height when using GaAsSb as opposed to InAlAs. This layer is intentionally left undoped in order to prevent gate current leakage to the S/D. A 300 Å, undoped, In_{0.52}Al_{0.48}As layer is used as a wide band gap layer. This layer is also left undoped to reduce gate leakage current. An undoped, 200 Å, GaAs_{0.51}Sb_{0.49} layer forms the 2DEG channel. A 3000 Å, lightly doped, In_{0.52}Al_{0.48}As layer is grown above the substrate in order to getter impurities from the substrate and provide a clean growth surface in the HIGFET layers. This layer also acts as a wider band gap layer and sets the pinchoff voltage for the GaAs_{0.51}Sb_{0.49} 2DEG channel.

Figures 3.3(b) through 3.3(f) summarize the SAG HIGFET fabrication steps. The SAG method uses the gate metal as a mask layer for S/D ohmic contact implant. This gate mask permits placing of the S/D regions as close to the gate as possible. Thus smaller area devices are obtainable - enabling increased device density and reduced carrier transit time from source to drain. Additionally, carrier recombination at the surface is reduced by decreasing the distance between the source and drain. Following growth, an O₂⁺ ion imp-

(a) HIGFET Device Profile

$\text{GaAs}_{0.51}\text{Sb}_{0.49}:\text{i}$, 50 Å
$\text{In}_{0.52}\text{Al}_{0.48}\text{As}:\text{i}$, 300 Å
$\text{GaAs}_{0.51}\text{Sb}_{0.49}:\text{i}$, 200 Å
$\text{In}_{0.52}\text{Al}_{0.48}\text{As}:\text{Be}$, $N_A = 10^{17} \text{ cm}^{-3}$, 3000 Å
Semi-Insulating InP Substrate

(b) Isolation Implant, Deposit W Layer on HIGFET Surface



(c) EBL Pattern Gate Metallization, Evaporate TiAu, Liftoff Excess TiAu, RIE W

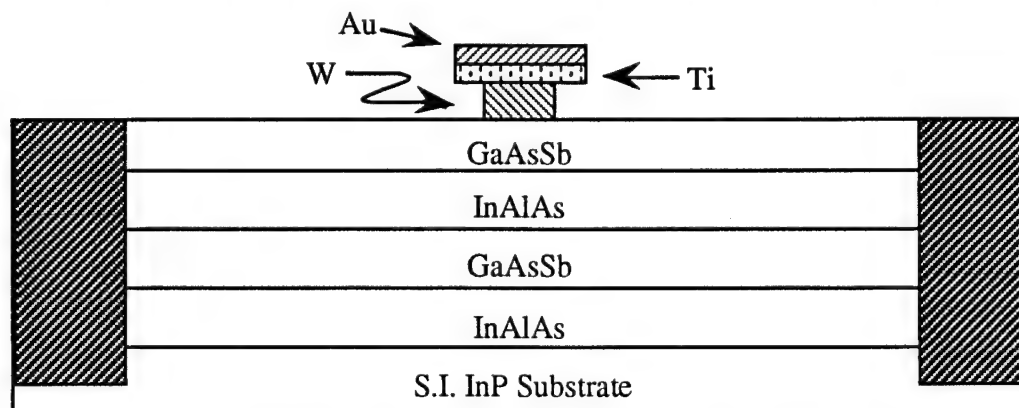
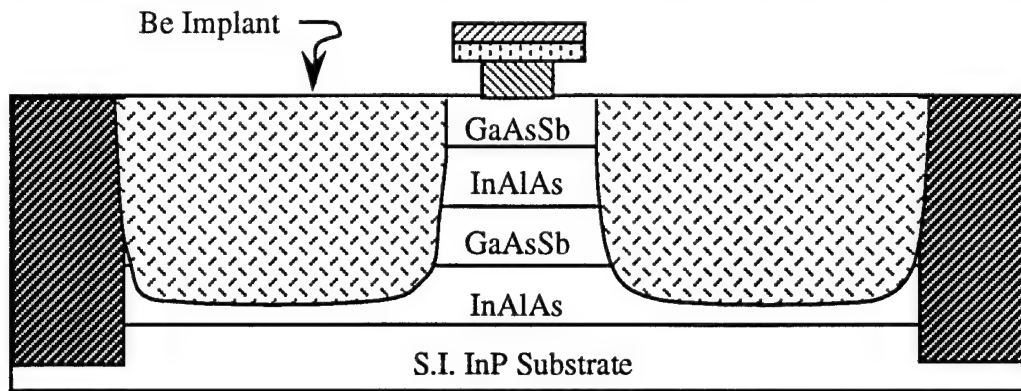
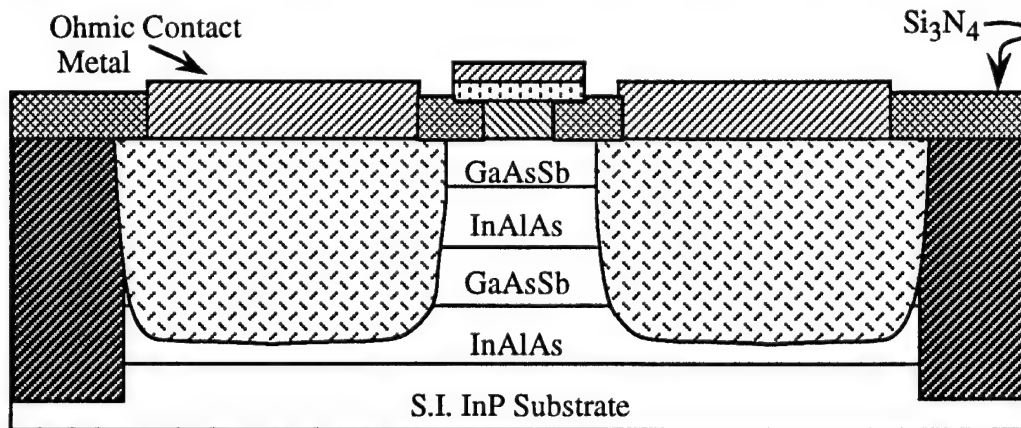


Figure 3.3. Self-aligned gate fabrication process for the InAlAs/GaAsSb HIGFET.

(d) Deposit Si_3N_4 , Pattern S/D, Implant S/D, RTA S/D Implant, Remove Si_3N_4



(e) Pattern S/D Contacts, Dep. Ohmic Contact Metal, Excess Metal Liftoff, RTA



(f) Deposit Silicon Nitride, Pattern & Etch Via Holes, Pattern Bonding Pad & Interconnects, Deposit Interconnect Metal, Liftoff Interconnect Metal

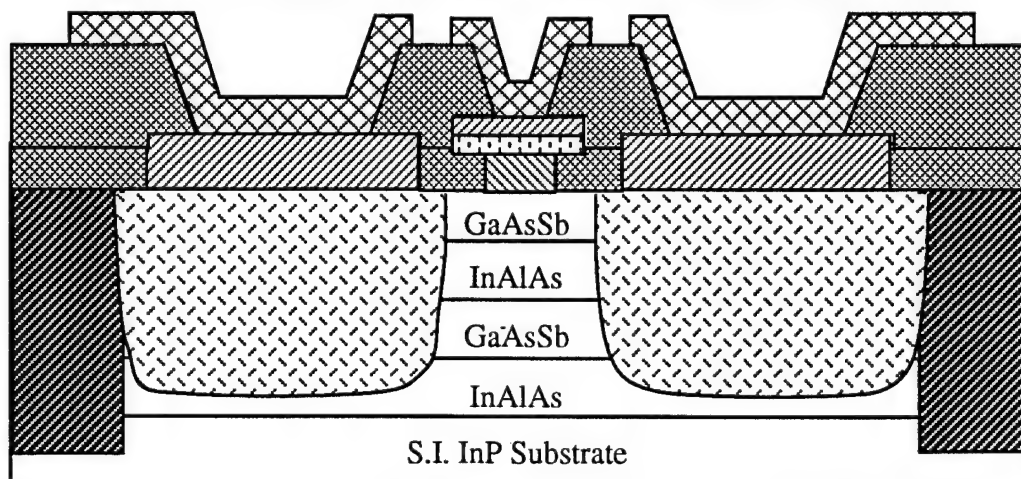


Figure 3.3 (cont.). Self-aligned gate fabrication process for the InAlAs/GaAsSb HIGFET.

lant is completed for device isolation. The surface is next cleaned and a layer of W is sputtered over the entire HIGFET surface as in Fig. 3(b). Next, electron beam lithography (EBL) is used to obtain submicron gate patterns for Ti/Au metallization (Fig. 3(c)). Excess Ti/Au is lifted off and the W layer is undercut using reactive ion etching (RIE). The W undercut prevents shorting between the gate and S/D regions. Once the gate metal is defined, a Be implant establishes the S/D regions for the p-channel HIGFET (Fig. 3(d)). A Si_3N_4 overlayer provides a shallow, uniform implant and suppresses sublimation of semiconductor elements at the GaAsSb surface during implant annealing. The S/D implant requires rapid thermal annealing (RTA) in order to activate the dopant species. Following S/D region definition, a new layer of Si_3N_4 is deposited over the HIGFET as in Fig. 3(e). The Si_3N_4 provides surface protection during ohmic contact alloying. The S/D ohmic contact regions are then established using conventional photolithography. The ohmic contact metal is deposited and then alloyed using RTA. Figure 3(f) shows the results of patterning and depositing second level metal for interconnect and wire bonding.

3.2.2 Ion Implantation of GaAsSb for Source and Drain Contacts. The ion implantation and anneal which form the S/D contact regions are critical since they affect: (1) the doping concentration for ohmic contact formation, (2) the GaAsSb surface on which the ohmic metal is deposited, and (3) the quality of the InAlAs/GaAsSb heterojunction. The implant conditions must first be determined including ion dose, and implant energy. Beryllium is attractive since it is less diffusive than Zn implants and has good activation in GaAs [16]. The implant anneal must occur at a temperature which provides maximum activation of the Be dopant species. In GaAs these RTA temperatures are typically 800 - 900 °C for 2 to 30 sec using RTA [16]. However, this maximum dopant activation occurs at a temperature higher than the growth temperature of InAlAs and GaAsSb (typically 500 °C) [17]. Therefore, the InAlAs/GaAsSb interface may degrade through cross diffusion of the semiconductor elements. Also, this temperature may cause outdiffusion of Ga, As or

Sb from the surface layer or In, Al or As species from the gate layers. The implant anneal time must be optimized as well. Thus the following items require determination for ion implantation of the S/D contact regions:

- (1) Implant energy and dose.
- (2) RTA temperature and time which provide high dopant activation with minimum InAlAs/GaAsSb heterojunction degradation.

3.2.3 The Role of Source and Drain Ohmic Contacts.

3.2.3.1 Impact of Ohmic Contacts on Operating Frequency. The choice of S/D ohmic contact metallization in the HIGFET affects: (1) frequency of operation and switching speed limits by altering the source and drain resistances (R_s and R_d), (2) the ease of SAG fabrication, and (3) device reliability. Consequently, efforts to improve HIGFET performance are controlled by ease of manufacturing, cost, and device reliability.

The fundamental importance of R_s and R_d with respect to frequency of operation and switching speed limits must be addressed. The unity current gain frequency, f_t , represents the frequency at which the short-circuit current gain falls to unity. Also, $1/f_t$ is approximately the carrier transit time through the channel for device switching in digital applications. Equation 3.1 relates the equivalent circuit components of the physical HIGFET device to f_t [18].

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (3.1)$$

where g_m is the device intrinsic transconductance, C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances respectively. The maximum frequency of oscillation, f_{max} , is the frequency at which the unilateral power gain goes to unity. This figure of merit is

important for microwave applications and is expressed in the common-source configuration as [18]:

$$f_{\max} = \frac{f_t}{2} \left[\frac{R_g + R_i + R_s}{r_{ds}} + 2\pi f_t R_g C_{gd} \right]^{-1/2} \quad (3.2)$$

where r_{ds} is the small signal, differential output resistance, R_i is the resistance from the gate to the channel and R_g is the resistance of the Schottky gate contact. Thus high values of source contact resistance will increase R_s and lower f_{\max} . Also, high values of R_s and R_d increase the resistance in series with the channel. Thus lower current flows for a given gate bias when R_s and R_d are increased.

3.2.3.2 Conventional Au/Zn/Au Ohmic Contacts to p-GaAsSb. Very little is published concerning p-type ohmic contacts to $\text{GaAs}_{1-x}\text{Sb}_x$ at or near lattice matched to InP ($0.45 \leq x \leq 0.55$) [19]. Consequently, investigation of conventional ohmic contacts to $\text{GaAs}_{1-x}\text{Sb}_x$ in this Sb composition range is important for future device development. Due to the lack of previous research, candidate metal-semiconductor systems for p-type ohmic contacts to p-GaAs_{1-x}Sb_x must be inferred from results on GaAs and GaSb. Conventional ohmic contacts to p-type GaAs use Au/Zn/Au. The ohmic contact forms by substitution of Zn on Ga sites (vacated by Ga outdiffusion). The outdiffusion of Ga atoms and indiffusion of Zn atoms ideally occurs on a one-to-one basis. However, this reaction is limited by Au interdiffusion and the formation of a liquid phase which limits Zn indiffusion [19]. The Au/Zn/Au system requires high temperature alloying (400 - 450 °C) with the inherent problem of vertical and lateral diffusion of the Au contact metal [20]. Excessive diffusion causes electrical shorting between the gate and S/D contacts, and non uniform scaling of R_s and R_d when device dimensions are reduced. Rapid thermal annealing of the Au/Zn/Au on p-GaAs produces a lower resistance ohmic contact ($\rho_c = 3.3 \times 10^{-6} \Omega\text{-cm}^2$, $N_A = 3 \times 10^{17} \text{ cm}^{-3}$) and limits Au diffusion compared with furnace annealing [20].

Furnace annealing of Au/Zn/Au on p-GaSb produces a minimum resistance ohmic contact ($\rho_c = 1 \times 10^{-5} \Omega\text{-cm}^2$, $N_A = 1 \times 10^{18} \text{ cm}^{-3}$) at 300 °C [21]. This specific contact resistance is rather high considering the low bandgap of GaSb compared to GaAs and the higher doping used in ref. 21 as opposed to ref. 20. Therefore, further investigation of alloying conditions appears necessary for Au/Zn/Au on p-GaAs_{1-x}Sb_x. No reports concerning electrical and microstructural properties of Au/Zn/Au on p-GaAs_{1-x}Sb_x are presently published to the authors knowledge. The following conclusions concerning the Au/Zn/Au ohmic contact to p-GaAs_{1-x}Sb_x result from the above discussion:

(1) RTA is promising for low resistance and short term thermal stability based on the results of p-GaAs.

(2) Furnace annealing does not appear lucrative for low resistance and thermal stability as per results on p-GaAs and p-GaSb.

(3) A study of the electrical and microstructural properties of the Au/Zn/Au metallization scheme on p-GaAs_{1-x}Sb_x is necessary to ensure process compatibility with GaAs-based devices, and to permit comparison with previous results on p-GaAs.

3.2.3.3 Thermally Stable, Refractory Ohmic Contacts to p-GaAsSb. The p-HIGFET is subject to thermal and bias stresses following ohmic metal deposition to the source and drain. Thermal stress may occur due to: (1) alloying of ohmic metallization in the complementary, n-channel HIGFET, (2) self-heating during operation, and (3) high temperature environments. The combination of thermal and bias stress can induce metal diffusion, electromigration, and mechanical stress. Consequently, S/D contacts must remain reliable and uniform in order to survive processing and deployment in systems using HIGFET-based ICs. For long term thermal stability, the development of a refractory S/D contact is warranted for the InAlAs/GaAsSb HIGFET.

Various thermally stable, refractory ohmic contacts have been investigated for p-GaAs [19,22,23], (with no known reports on p-GaAs_{1-x}Sb_x). Refractory S/D ohmic contacts using Ti/Pt/Au are attractive compared with W-based contacts since sputtering is required for W. Well defined contact edges are difficult to obtain using conventional photolithography with sputtered W. Also, Ti/Pt/Au is evaporated - allowing deposition of all ohmic contact metal elements in one evaporation chamber. Ti/Pt/Au has been used extensively as a thermally stable, refractory gate contact in III-V FET devices and as an ohmic contact to HBT devices. Ti/Pt/Au is thus a refractory contact compatible with conventional III-V device processes. Therefore, Ti/Pt/Au should be investigated as a nonalloyed ohmic contact to p-GaAs_{1-x}Sb_x.

A nonalloyed Ti/Pt/Au contact to p-GaAs_{1-x}Sb_x is possible based on the results of nonalloyed ohmic contact studies on p-GaAs and p-GaSb. Nonalloyed ohmic contacts have been formed on epitaxially grown p-type GaAs (using Ti/Pt, $\rho_c = 3 \times 10^{-6} \Omega\text{-cm}^2$) [24] and p-GaSb (using AuBe, $\rho_c = 3.2 \times 10^{-7} \Omega\text{-cm}^2$) [25]. These nonalloyed ohmic contacts to GaAs and GaSb used heavy doping of the semiconductor layer with $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ in both cases. The potential to use a nonalloyed, refractory Ti/Pt/Au S/D contact is more lucrative in GaAs_{1-x}Sb_x than GaAs since the bandgap is lower. Sintering of Ti/Pt ohmic contacts on epitaxially grown p-GaAs further reduces the contact resistance from the as-deposited value [24]. Consequently, sintering of Ti/Pt/Au should improve ohmic contact resistance to p-GaAs_{1-x}Sb_x. In the event that alloying is needed to form a refractory ohmic contact, metal layers are needed which contain elements that further lower the metal-semiconductor barrier height and increase the GaAs_{1-x}Sb_x acceptor concentration.

Formation of a refractory, alloyed ohmic contact to p-GaAs_{1-x}Sb_x will require many of the same mechanisms used in alloyed p-GaAs ohmic contacts. Contact resistance lowering in p-GaAs ohmic contacts occurs through gettering of Ga atoms from the semiconductor surface [19]. The Ga atoms are then replaced by atoms from dopant

elements (Be, Zn, Mn, Mg, etc.) in the contact metal. Considerable effort is dedicated to refractory, alloyed ohmic contacts on n-GaAs, formed by adding a layer of In to the metallization [26,27]. The addition of In causes the formation of an $\text{In}_x\text{Ga}_{1-x}\text{As}$ surface layer and a reduced metal-semiconductor energy barrier height. This $\text{In}_x\text{Ga}_{1-x}\text{As}$ surface layer is formed by the outdiffusion of surface Ga and the indiffusion of In atoms to Ga lattice sites. No known effort has been reported in the pursuit of a refractory, In-based ohmic contact to p-GaSb or p-GaAs $_{1-x}\text{Sb}_x$. However, addition of In to non-refractory ohmic contacts of AuBe/Ag/Au on p-GaAs significantly reduced contact resistance [28].

The Ti/Pt/Au system should provide a thermally stable, refractory ohmic contact to GaAs $_{1-x}\text{Sb}_x$ through the addition of a dopant element and/or an In layer. In the Ti/Pt/Au system, Ti promotes metal adhesion to III-V compounds and getters Ga in GaAs [23,24]. Therefore, the Ti layer should promote Ga outdiffusion and allow a highly doped surface layer with a lower barrier height. The Pt behaves as a diffusion barrier to Au; enhancing thermal stability. The Au layer is necessary for low contact resistance and device interconnection to IC packages. Thus selection of the doping and/or bandgap-narrowing elements is necessary with the Ti/Pt/Au metal used for electrical contact to the alloyed region. Based on the above discussion, the following approach results for obtaining a thermally stable, refractory ohmic contact to p-GaAs $_{0.51}\text{Sb}_{0.49}$:

- (1) Determine if a nonalloyed (or sintered), refractory ohmic contact is possible using Ti/Pt/Au.

- (2) If a nonalloyed refractory ohmic contact is not possible, develop an alloyed ohmic contact incorporating layers with both a refractory barrier metal and an acceptor dopant and/or a barrier height lowering element (i.e. In/Ti/Pt/Au, Be/In/Ti/Pt/Au, etc.).

3.3. Research Outline

The primary objective of this dissertation research is to obtain a low resistance, thermally stable, ohmic contact applicable to p-type, InAlAs/GaAsSb SAG HIGFETs. Research on p-GaAs_{1-x}Sb_x ($0.45 \leq x \leq 0.55$) is accomplished versus n-GaAs_{1-x}Sb_x to focus the research on a single material type, and to publish p-type ohmic contact results which are less reported compared with n-type. The objective is initially approached through determination of the thermal stability of the InAlAs/GaAsSb HIGFET. Also, the temperature dependence of the direct band gap energy and impurity states are investigated in Be-doped GaAs_{1-x}Sb_x in order to quantify these parameters for empirical and theoretical studies. Next, ion implanted GaAs_{1-x}Sb_x layers are characterized in order to optimize dopant activation in the S/D contact regions without damaging the InAlAs/GaAsSb heterojunction. After the ion implantation step is optimized, Au/Zn/Au and Ti/Pt/Au ohmic contacts are deposited, and characterized electrically and microstructurally. Microstructural characterization including secondary ion mass spectroscopy (SIMS), auger electron spectroscopy (AES), x-ray diffraction (XRD), cross-sectional transmission electron microscopy (XTEM), scanning electron microscopy (SEM), photoluminescence (PL) and atomic force microscopy (AFM) are used to determine ion implantation and metal-semiconductor interactions. Experimental results will demonstrate improved electrical performance for the InAlAs/GaAsSb HIGFET using ion implanted source and drain regions coupled with nonalloyed ohmic contacts.

Advance emphasis is placed on the fact that this research effort does not ultimately produce a sub-micron, SAG HIGFET. Such an effort is beyond the scope of individual, independent research emphasizing source/drain implantation and contacts. A SAG process is particularly difficult due to development of the proper gate geometry using electron beam lithography. Consequently, the goal of this dissertation is to produce and characterize

building blocks which give the InAlAs/GaAsSb HIGFET a "push" in the direction of SAG technology.

3.4 Chapter III Summary

The research objectives of subsequent chapters were overviewed: obtaining reliable, low resistance, ohmic contacts to ion-implanted p-GaAs_{1-x}Sb_x at or near lattice matched InP ($0.45 \leq x \leq 0.55$). This research will improve technology applicable to self-aligned gate, InAlAs/GaAsSb HIGFETs. HIGFET advantages, operating principles, and applications were presented in order to compare the HIGFET with other III-V FET technologies. A problem statement was given, focusing on the issues of ion implantation and ohmic contact formation for the self-aligned, InAlAs/GaAsSb HIGFET. This problem statement demonstrates that investigation of both alloyed and nonalloyed ohmic contacts to p-GaAs_{1-x}Sb_x is warranted in order to obtain HIGFET design goals. This research thus focuses on issues which advance novel materials for improved III-V FETs.

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IV. The Effect of Temperature on InAlAs/GaAsSb HIGFET Epilayers and p-GaAsSb

4.1 Introduction

The $\text{GaAs}_{1-x}\text{Sb}_x$ semiconductor has recently been grown on InP substrates for use in electronic and optoelectronic applications [1-5]. A wide variety of III-V heterostructure devices is achieved by incorporating $\text{GaAs}_{1-x}\text{Sb}_x$ epilayers with InAlAs or InGaAs. The $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction has a high valence band discontinuity [1] which enables superior hole confinement in p-channel HIGFETs [2], and high current gain in n-p-n heterojunction bipolar transistors (HBTs) [3]. The $\text{GaAs}_{1-x}\text{Sb}_x/\text{In}_y\text{Ga}_{1-y}\text{As}$ system was investigated in superlattices [4] and heterojunction diodes [5]. These efforts represent first attempts to bridge the gap between materials growth and device generation. Still, little is known concerning the thermal limitations of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction and the thermal properties of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ material used in these devices. Thermal limitations and material properties are important parameters in device design, testing and fabrication.

Thermal cycling of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction in a HIGFET structure determines the allowable temperature limit for device fabrication. Maturation of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET to complementary technologies requires progression to self-aligned gate (SAG) devices. The SAG process uses thermal cycling during a number of process steps including implanted dopant activation and ohmic contact alloying. Section 4.2 establishes the upper temperature limit for both SAG and recessed-gate (RG) epilayers and explains the sources of structural degradation.

Accurate modeling of device designs requires knowledge of both the direct band gap energy (E_g) and impurity energy levels as a function of temperature. Optical spectroscopy is used in Section 4.3 to investigate both E_g and impurity related energy

levels for Be-doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. In Section 4.4 the results of Section 4.3 are used to simulate the energy band diagram and quantized energy levels for a $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET structure lattice matched to InP. The simulated results are compared with the experimental PL results obtained in Section 4.1.

4.2 Rapid Thermal Annealing Effects on InAlAs/GaAsSb HIGFET Epilayers*

4.2.1 Sample Preparation and Rapid Thermal Annealing Conditions. The samples were grown in a Varian Gen-II MBE system on semi-insulating InP:Fe substrates oriented in the (100) direction. The nominal growth temperature and rate was 500 °C and 0.8 monolayers/sec for both the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers. Two $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET structures were used in this study. The layer profiles are shown in Figure 4.1(a) for a recessed gate and Figure 4.1(b) for a self-aligned gate structure. The thickness and doping concentration of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface layer determines the HIGFET gate configuration. The first structure has a 50 Å, undoped, $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. Thus a very narrow, low band gap surface layer is realized for later ion implantation of source and drain regions aligned to the gate. The layer is undoped to lessen gate leakage effects. The second structure has a 500 Å, Be-doped, $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer with a $1 \times 10^{19} \text{ cm}^{-3}$ doping concentration. This layer profile is designed for a recessed gate HIGFET device since the highly doped, narrow band gap cap layer is desirable for source and drain contacts. This cap layer is etched completely prior to gate metal deposition. The samples are henceforth referred to as the "50 Å" or "500 Å" sample based on the thickness of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface layer. Both samples have a 200 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel between $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers. A 10-period, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ superlattice is located above the substrate and serves as a buffer layer prior to HIGFET growth.

* Results from this section were presented and published at the *21st International Symposium on Compound Semiconductors*, reference [6].

(a) Self-Aligned Gate, "50 Å" Sample

GaAs _{0.51} Sb _{0.49} :i, 50 Å
In _{0.52} Al _{0.48} As:i, 300 Å
GaAs _{0.51} Sb _{0.49} :i, 200 Å
In _{0.52} Al _{0.48} As:i, 3000 Å
In _{0.52} Al _{0.48} As:i/In _{0.53} Ga _{0.47} As:i SL, 30/30 Å, 10 Periods
Semi-Insulating InP Substrate

(b) Recessed Gate, "500 Å" Sample

GaAs _{0.51} Sb _{0.49} :Be, 1x10 ¹⁹ cm ⁻³ 500 Å
In _{0.52} Al _{0.48} As:i, 300 Å
GaAs _{0.51} Sb _{0.49} :i, 200 Å
In _{0.52} Al _{0.48} As:i, 3000 Å
In _{0.52} Al _{0.48} As:i/In _{0.53} Ga _{0.47} As:i SL, 30/30 Å, 10 Periods
Semi-Insulating InP Substrate

Figure 4.1. Layer profiles of the two In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} samples: (a) self-aligned gate and (b) recessed gate epilayers. The GaAs_{0.51}Sb_{0.49} surface layer thickness designates the sample name.

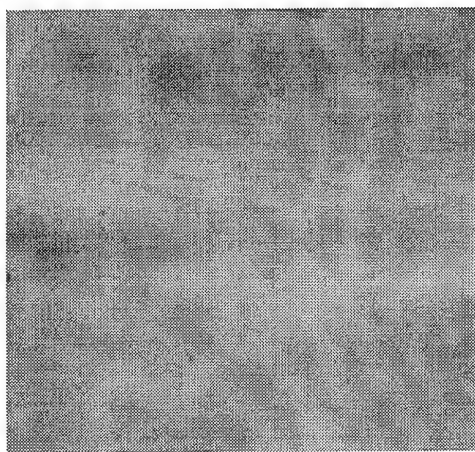
Rapid thermal annealing was performed in a Heatpulse 210 system under a 10 standard cubic centimeters per minute (sccm) flow of forming gas (95% Ar, 5% H₂). Both the 50 Å and 500 Å sample were placed inside a graphite ring, underneath a GaAs wafer during RTA in order to limit potential As sublimation from the samples. Samples were

subjected to RTA at temperatures of 600, 700 and 800 °C for 10 seconds in order to establish a maximum annealing temperature which maintains the heterojunction integrity. Separate samples from neighboring wafer pieces were used at each temperature.

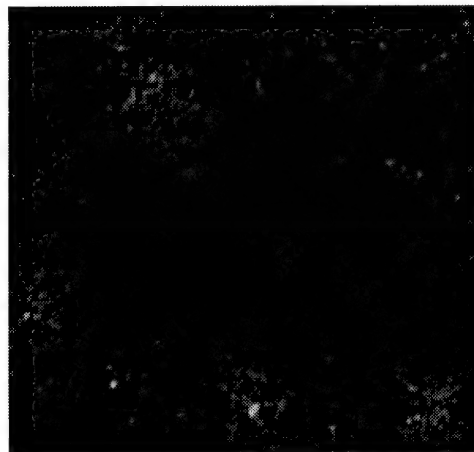
4.2.2 Optical Microscopy and Profilometry Results. The structural quality of the samples was monitored using optical microscopy, surface profilometry and photoluminescence. Optical images were obtained with a Zeiss microscope at a 200X magnification using a combination of Nomarski, bright, and dark field imaging. The surface profiling was performed using a Tencor Alpha Step 250 system with a resolution of 20 Å. Photoluminescence (PL) measurements were performed at a temperature of 4 K using a dual-mode Ar laser source with 4888 Å and 5145 Å lines. Luminescence was monitored with a 1.2 m spectrometer and a Ge photodetector cooled by liquid N₂.

Following RTA, optical micrographs and surface profilometry were used to determine the morphology of the GaAs_{0.51}Sb_{0.49} surface. The optical micrograph images are shown in Figures 4.2(a-d). Figure 4.2(a) is imaged in light field while Figures 4.2(b-d) are in dark field. The as-grown sample surfaces were specular with minimal surface defects as shown in Figure 4.2(a). The surface of the 500 Å sample was unchanged following RTA at 600 and 700 °C. After an 800 °C anneal the 500 Å sample demonstrated a uniform roughness over the entire surface (Figure 4.2(b)). The profilometer measurements showed a peak-to-valley roughness of approximately 100 Å. The surface of the 50 Å sample was smooth following RTA at 600 °C. However the surface exhibited circular patterns following annealing at 700 °C as in Figure 4.2(c). The circular patterns ranged from 50 to 200 µm in diameter. The surface of the 50 Å sample produced a continuum of elongated, ridge-like, patterns following RTA at 800 °C. The peak-to-valley height of the roughness following the 800 °C anneal was 300 Å as per profilometer measurements. The peaks of the ridge-like patterns are separated by approximately 5 to 10 µm. Both samples had catastrophic surface morphology degradation at 800 °C - rendering

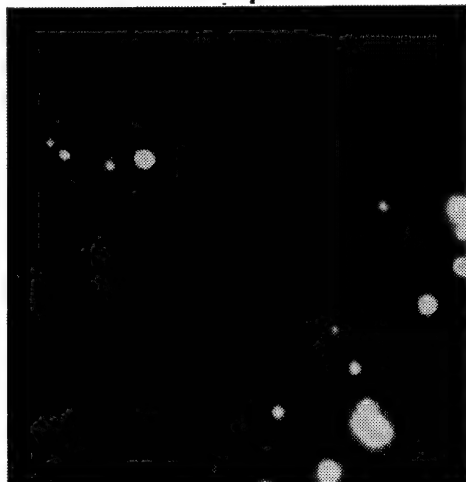
(a) As-grown, Light Field



(b) Post 800 °C, 10" RTA
500 Å Sample



(c) Post 700 °C, 10" RTA
50 Å Sample



(d) Post 800 °C, 10" RTA
50 Å Sample

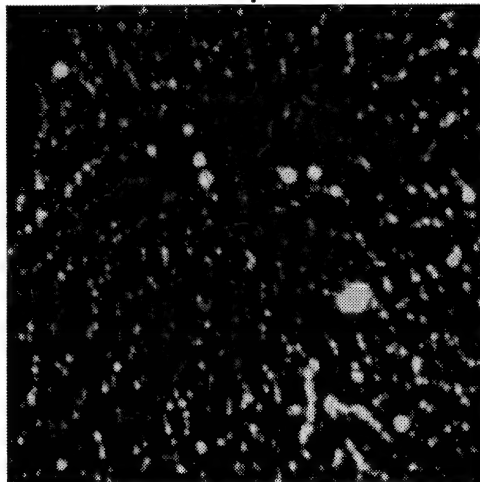


Figure 4.2 Optical micrographs of the surface of two InAlAs/GaAsSb HIGFET samples. The micrograph in (a) was taken in light field image while (b - d) are dark field images. The image boundaries represent 300 μm per side.

further fabrication untenable. Surface morphology considerations thus set a maximum anneal temperature limit of 600 °C and 700 °C respectively for the 50 Å and 500 Å HIGFET structures when 10 second anneals are used.

The samples were annealed at 600 °C with varying anneal times to determine the sensitivity of the surface and heterojunction to anneal time. Both samples were annealed for 5 minutes. The surface morphology for both samples was unchanged following each of these anneal times.

4.2.3 Photoluminescence Results. Photoluminescence measurements were taken at $T = 4$ K to determine the quality of the GaAsSb channel after subjection to increasing RTA temperature. The PL peak energy and linewidth from the e_1 -hh₁ (first electron to first heavy hole) free exciton transition were measured following each thermal cycle. The GaAs_{0.51}Sb_{0.49} surface layers were first removed using wet chemical etching in H₃PO₄:H₂O₂:H₂O:L-Tartaric Acid (1:1:150:0.4) in order to increase the intensity of the luminescence emitted from the heterojunction. The PL results are shown in Figures 4.3(a) and 4.3(b). The peak energy and linewidth increased for both samples as the RTA temperature was increased to 600 °C and 700 °C (10 second anneal times were used). No PL signal was observed from the In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} heterojunction in either sample following the 800 °C, 10 second, RTA. Both samples exhibited the same trends in PL peak energy and linewidth with respect to RTA temperature which is encouraging from a corroboration standpoint. Thus catastrophic degradation of the heterojunction (as well as the sample surfaces) occurred at 800 °C.

4.2.4 Secondary Ion Mass Spectroscopy Results. SIMS measurements were obtained for the In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} HIGFET samples. The samples were analyzed using a Cameca IMS-3f system. Sample surfaces were sputtered with a Cs⁺ primary ion beam, raster scanned over a 125 x 125 μm² area with an 8 keV impact energy; negative ions were monitored.

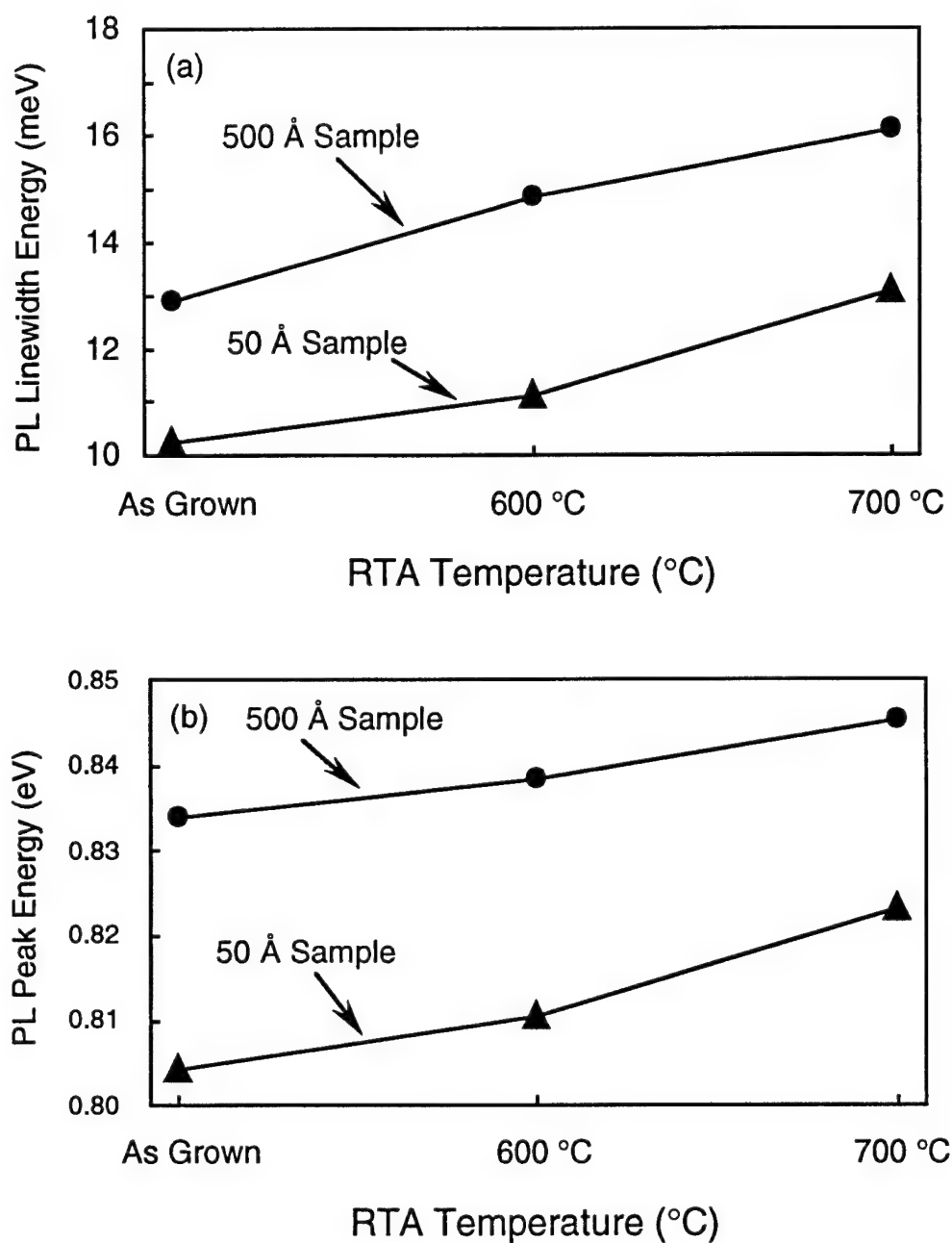


Figure 4.3. Photoluminescence energy versus RTA temperature for the e_1-hh_1 free exciton transition in a $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET structure: (a) linewidth energy (full width at half maximum) and (b) peak emission energy. Ten second anneals were used at each RTA temperature. PL was taken after each RTA cycle at $T = 4$ K. The $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel layer thickness is nominally 200 Å. Separate samples were used at each temperature.

The SIMS results are illustrated in Figures 4.4 for the HIGFET samples capped with a 50 Å layer of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. SIMS spectra were taken as-grown, and following rapid thermal annealing for 10 seconds at 600, 700 and 800 °C. In the as-grown case the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers are clearly delineated by following the Sb, In and Al element traces. The center of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ gate layer is located approximately 200 Å beneath the surface as evidenced by the first drop off in the Sb secondary ion emission and the first peak in the In and Al element profiles. Likewise, the center of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel layer is positioned approximately 450 Å from the surface and is represented by a peak in the Sb, and minima in the In and Al elements. Following annealing at 600 °C the spectra resemble the as-grown case where the interfaces between the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers are well defined. At 700 °C considerable cross diffusion occurred as indicated by broadening of the As, Sb, In and Al element traces. The Sb signal increased significantly at depths below 600 Å, demonstrating indiffusion into the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer from the channel. The $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel layer was still detectable by the slight dips in the In and Al signals at depths between 450 and 500 Å. The diffusion process continues at 800 °C as evidenced by a decrease in the magnitudes of the slopes of the As, Al, In and Sb signals. These SIMS results demonstrate deterioration of the SAG epilayers initiates at 700 °C and is complete at 800 °C.

Figure 4.5 contains the SIMS spectra for the HIGFET capped with 500 Å of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The thicker $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer is observed by the flat minima in the In and Al signals near the surface of the as-grown profile. The gate, channel and buffer layers are defined by the opposite trends in the In and Al signals versus the Sb signal as in Figure 4.4. Little change was observed in the elemental profiles following RTA at 600 °C and 700 °C. Therefore, the structural integrity of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ epitaxial layers is maintained to 700 °C. After the 800 °C RTA the interfaces between the

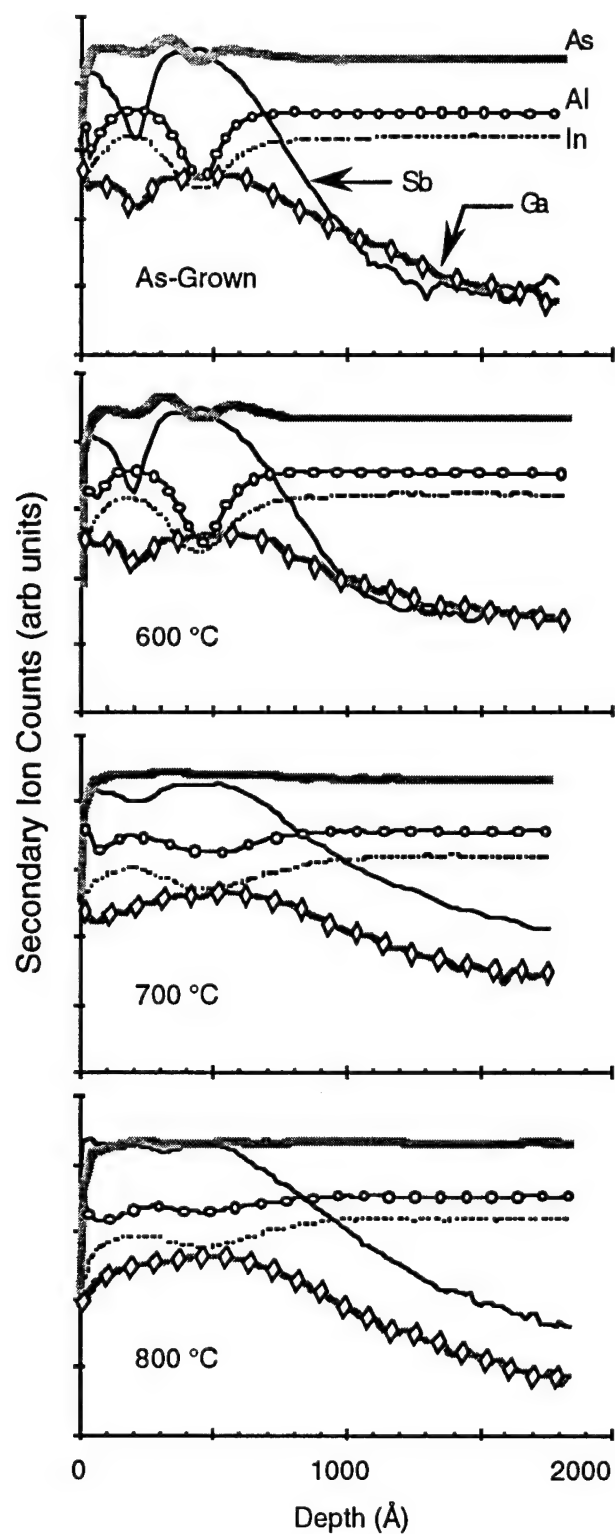


Figure 4.4. SIMS depth profiles for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 50 Å, $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. The spectra were measured as-grown, and following RTA for 10 seconds at 600 °C, 700 °C and 800 °C.

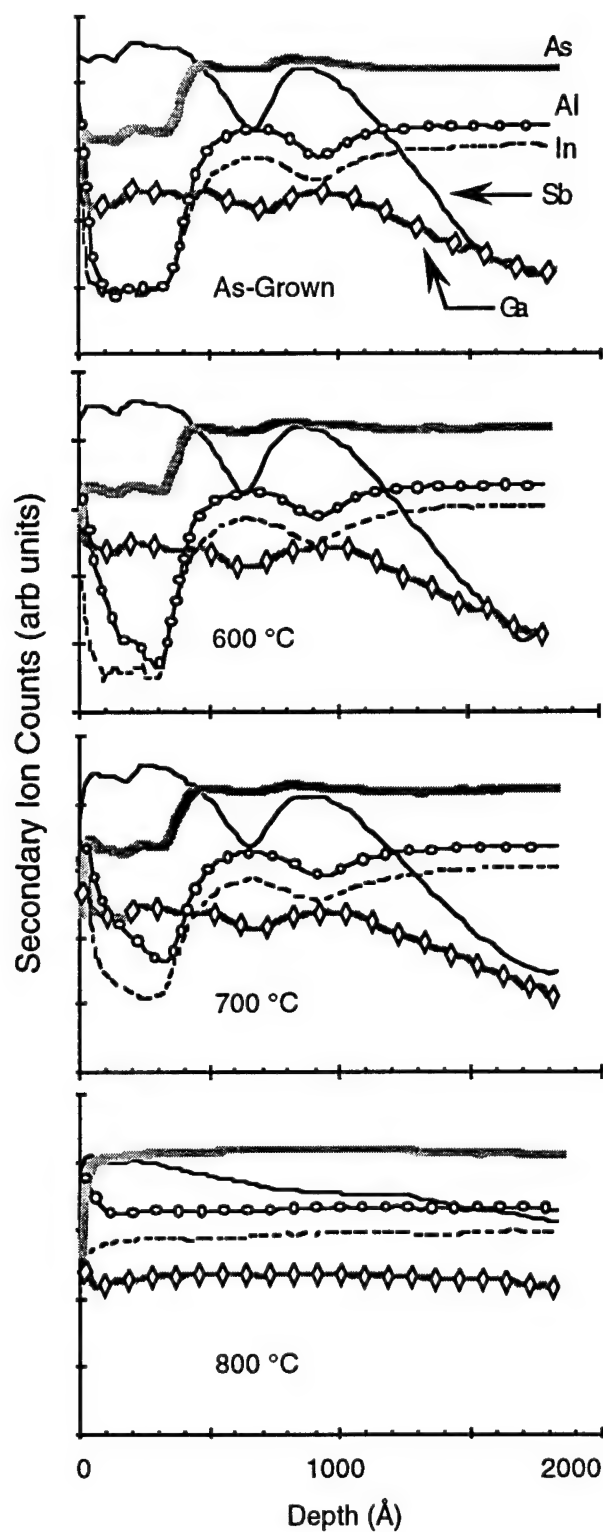


Figure 4.5. SIMS depth profiles for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 500 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. The spectra were measured as-grown, and following RTA for 10 seconds at 600 °C, 700 °C and 800 °C.

individual layers are no longer identifiable due to considerable cross diffusion of the III-V elements. A comparison of the SIMS profiles in Figures 4.4 and 4.5 indicates elemental diffusion is more severe at 700 °C for the 50 Å sample than the 500 Å sample. Also, both samples have no clearly definable $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction region following RTA at 800 °C. The loss of epilayer integrity at 800 °C is more substantial in the recessed gate sample as represented by the deep penetration of elements from $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap and channel epilayers.

4.2.5 Auger Electron Spectroscopy Results. Auger electron spectroscopy was conducted on the 50 and 500 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction samples. Both scanning Auger surface analysis and elemental depth profiling were performed. A Perkin-Elmer PHI 660 Scanning Auger Microanalyzer was used. The samples were sputtered with a 20 nA, 4 keV Ar^+ primary ion beam. The ion beam was raster scanned over a 200 μm x 200 μm analysis crater. In each sputter depth profile Ga, As, Sb, In, Al, As and O were monitored in a sputter/analysis mode. The AES data was collected from the center of the crater over an area approximately one-tenth of the total crater area. The focused electron beam used for this study had an acceleration energy of 5 keV at a current of approximately 1 μA .

Surface scanning Auger microanalysis was performed on the 50 Å sample in order to identify the source of the circular regions observed following RTA at 700 °C (Figure 4.2(c)). In the surface scanning mode, no sputtering is performed. Instead, the probe electron beam is raster scanned over the surface and Auger electron emission is monitored. The escape depths of Auger electrons in III-V semiconductor materials are typically within 10 Å to 15 Å of the sample surface [7]. Therefore, the scanning AES method is highly sensitive to surface element identification. The results of the surface analysis are shown in Figure 4.6 along with a scanning electron micrograph of the circular regions.

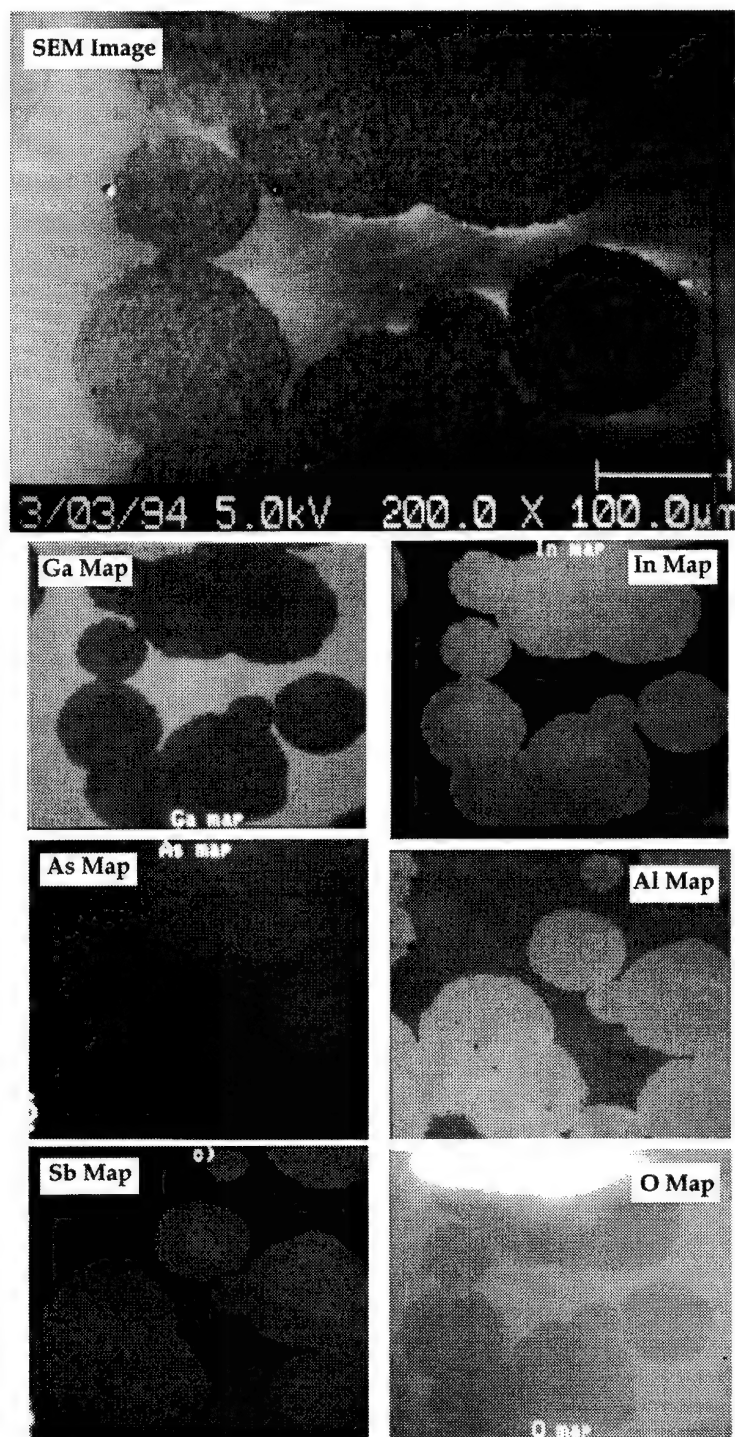


Figure 4.6 SEM and Scanning Auger micrographs of an InAlAs/GaAsSb HIGFET surface with a 50 Å GaAs_{0.49}Sb_{0.51} cap layer. The micrographs were taken following RTA at 700 °C for 10 seconds.

The SEM image delineates specular, non-degraded, surface regions and circular, degraded, surface regions. AES elemental maps for Ga, As, Sb, In, Al and O are placed beneath the SEM micrograph. Areas of high elemental concentration are depicted as lighter regions while darker areas indicate a lower concentration. The contrast between the light and dark regions provides a measure of the difference in element concentration in the circular and field regions. The AES micrographs prove these two regions vary in relative elemental concentration. The circular regions are rich in Sb, In and Al, and deficient in Ga and O. The two different surface areas are henceforth referred to as the "*field*" and "*circular*" regions. The circular surface patterns were observed on the 50 Å sample following 700 °C annealing but not on the 500 Å sample. A comparison of elemental diffusion in the two regions permits determination of the degradation mechanisms in the HIGFET structure. AES depth profiling results from the two regions are subsequently compared.

Figures 4.7(a-f) illustrate the AES depth profiles for the 50 Å sample. Each figure demonstrates the profile for a single element as-grown and following a ten second anneal at 600, 700 or 800 °C. The spectra begin at the GaAs_{0.51}Sb_{0.49} cap layer surface. There are two spectra for the 700 °C RTA temperature in each figure. One of the 700 °C spectra was obtained in the field region (open circle) while the other spectra was measured in the circular region (dark circle). The as-grown spectrum for each element demonstrates that the cap, gate and channel layers are well defined. The Ga, As and Sb spectra of Figures 4.7(a-c) chronicle deterioration of the cap and channel layers following RTA. The Ga spectra shows the 600 °C RTA produced no measurable diffusion. The 700 °C RTA produced a slightly lessened Ga signal intensity in the gate and channel layers of the field region. In the circular region considerable diffusion of Ga occurred. The Ga from the cap layer diffused inward while the channel Ga diffused both outward and inward. The Ga profile following the 800 °C RTA is very similar to that of circular region. The As profile

remained essentially the same after 600 °C RTA and was unchanged in the field region after a 700 °C RTA. The spectrum in the circular region and following 800 °C RTA exhibited As indiffusion into the channel layer. The Sb contours are consistent as-grown, post 600 °C RTA, and in the field region. The Sb content increased in the gate layer in the circular region at 700 °C and continued to increase after RTA at 800 °C. The Sb diffused from the channel region towards the surface as opposed to diffusing both inward and outward as in the Ga case. The In spectra of Figure 4.7(d) revealed diffusion from the gate layer into both the cap and channel layers. Also, In from the buffer layer spread into the channel layer. The Al diffused in a manner similar to the In whereby the cap layer and channel layers increased in Al content in both the circular region at 700 °C and following RTA at 800 °C. The oxygen spectra are included for completeness. The O profiles demonstrate that oxidation of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface is limited to a depth of approximately 30 Å irrespective of anneal temperature. A 30 Å, oxidized $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface is similar to the thicknesses of native oxide layers on GaAs which are approximately 25 Å [8].

The AES surface maps demonstrated that the circular regions are rich in Sb, In and Al, and deficient in Ga and O. The surface results for the circular and field regions concur with the near surface AES depth profiles in Figure 4.7. The AES profile exhibited a higher surface Sb concentration in the circular region than in the field region. In the circular region, Ga outdiffusion is coincident with the Sb surface clustering. The circular region thus appears caused by simultaneous indiffusion of surface Ga with outdiffusion of channel layer Sb, followed by movement of unbonded Sb surface atoms to the Sb-rich circular regions. The absence of surface Ga in the circular regions is further verified by a deficiency of O since excess surface Ga would readily form Ga oxides. The As content in the channel increased due to preferential indiffusion from the gate layer as opposed to the buffer layer. Surface deterioration in the circular regions occurred through outdiffusion of In and Al from the gate layer.

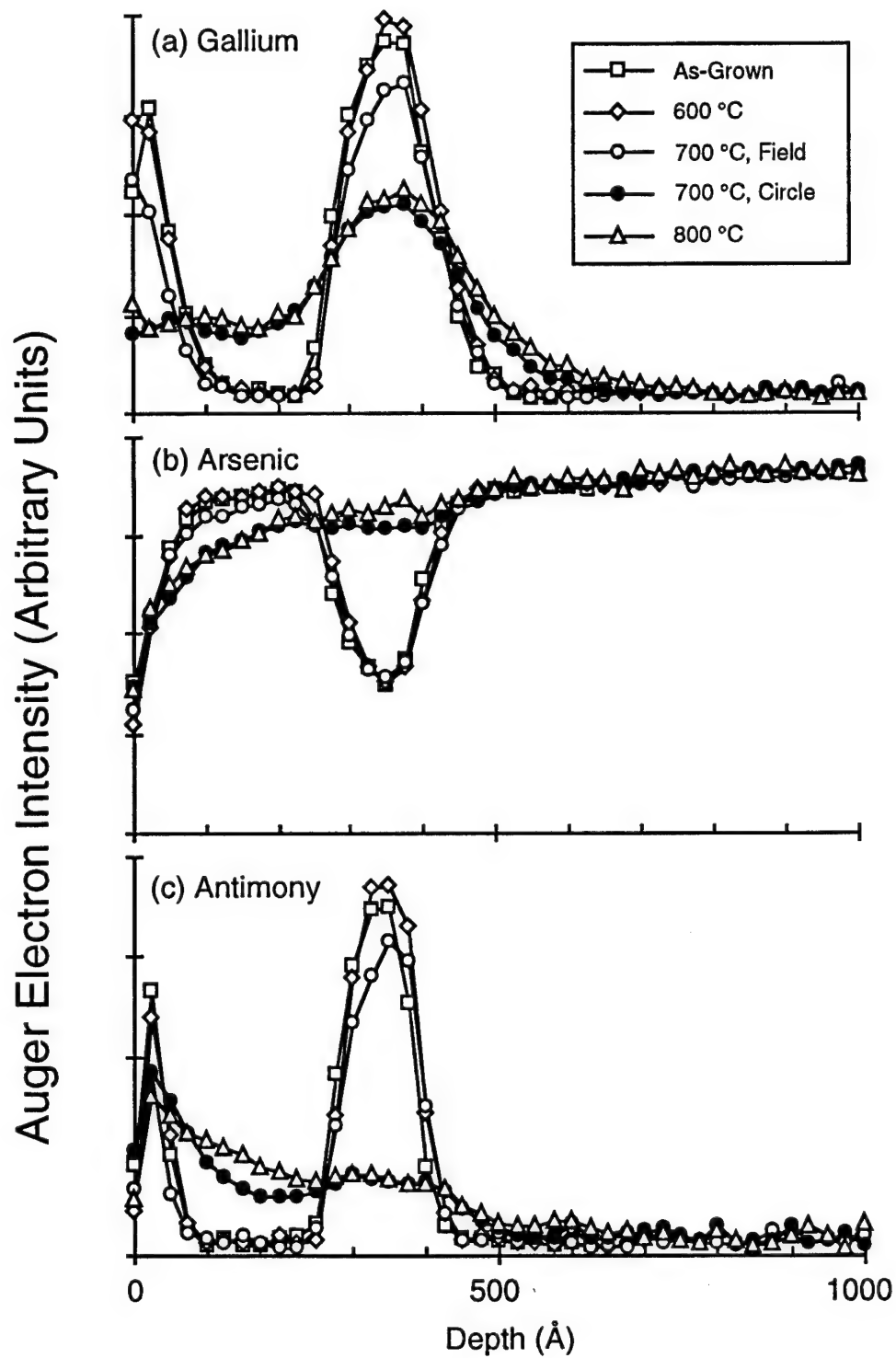


Figure 4.7. AES depth profile for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 50 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. The spectra were measured as-grown, following rapid thermal annealing for 10 seconds at 600 °C, 700 °C (field and circular regions) and 800 °C. The (a) Ga, (b) As, and (c) Sb depth profiles are shown.

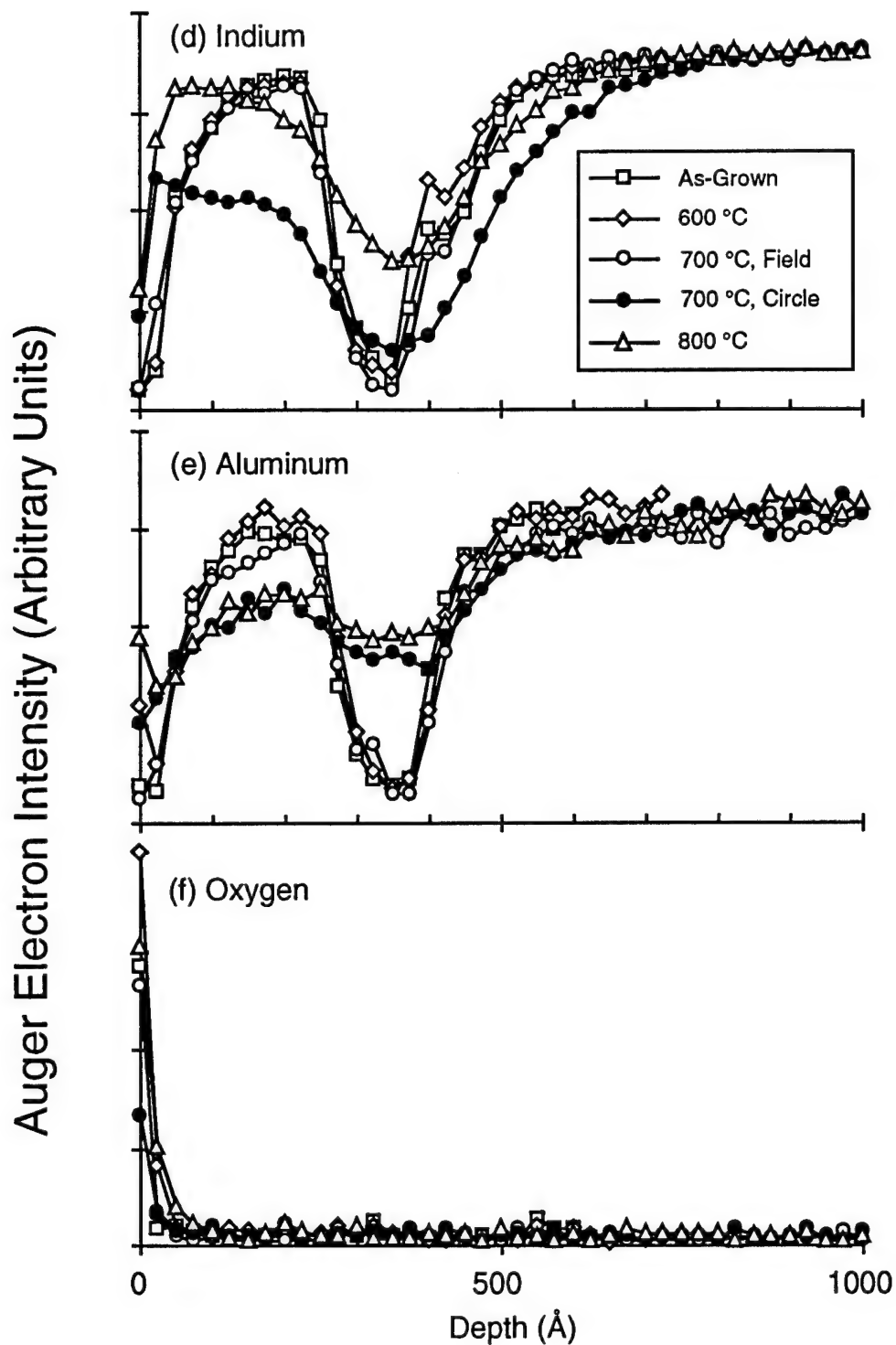


Figure 4.7(cont.). AES depth profile for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 50 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. The spectra were measured as-grown, following rapid thermal annealing for 10 seconds at 600 °C, 700 °C (field and circular regions) and 800 °C. The (d) In, (e) Al, and (f) O depth profiles are shown.

AES depth characterization of epilayers in the 500 Å sample is illustrated in Figure 4.8. Little elemental diffusion is evidenced in the plots for the 600 and 700 °C anneals. These results are consistent with the optical micrographs of Figure 4.2(a), showing a specular surface on the 500 Å sample following RTA at 700 °C. The depth scale in Figure 4.8 was increased over that of Figure 4.7 to account for both the thicker GaAs_{0.51}Sb_{0.49} cap layer and deep diffusion of some semiconductor elements. Indiffusion of Ga was evidenced by the decrease in the Ga signal at the surface as the RTA temperature was increased to 700 °C. Indiffusion of Ga was highly evident following the 800 °C anneal. The Ga level in the cap layer decreased considerably and was essentially uniform to a depth of 1000 Å. A Ga signal was detectable at least 1000 Å into the In_{0.48}Al_{0.52}As buffer layer. Thus the large Ga concentration presented by the 500 Å cap layer produced considerably more indiffusion than the 50 Å cap layer. The As concentration in the GaAs_{0.51}Sb_{0.49} channel layer increased. Arsenic outdiffusion towards the surface appears as an increase in the As concentration in the cap layer. The Sb profiles are reduced to less than half of the as-grown values in the cap layer with a slight reduction observed in the channel. Little Sb indiffusion from the channel layer into the buffer layer was evidenced. The In spectrum showed outdiffusion from a depth 1800 Å past the channel/buffer layer interface. The combination of outdiffusion from the gate and buffer layers produced a large amount of In congregation at the semiconductor surface. The Al outdiffusion appeared less severe than that of the In - the Al in the near surface region mostly coming from the gate layer. The oxygen contours again show oxidation occurred only at the surface except for slightly deeper penetration following the 700 °C anneal. These AES depth profile results demonstrate that the thicker GaAsSb cap layer prevents the onset of microstructural degradation to temperatures up to 700 °C.

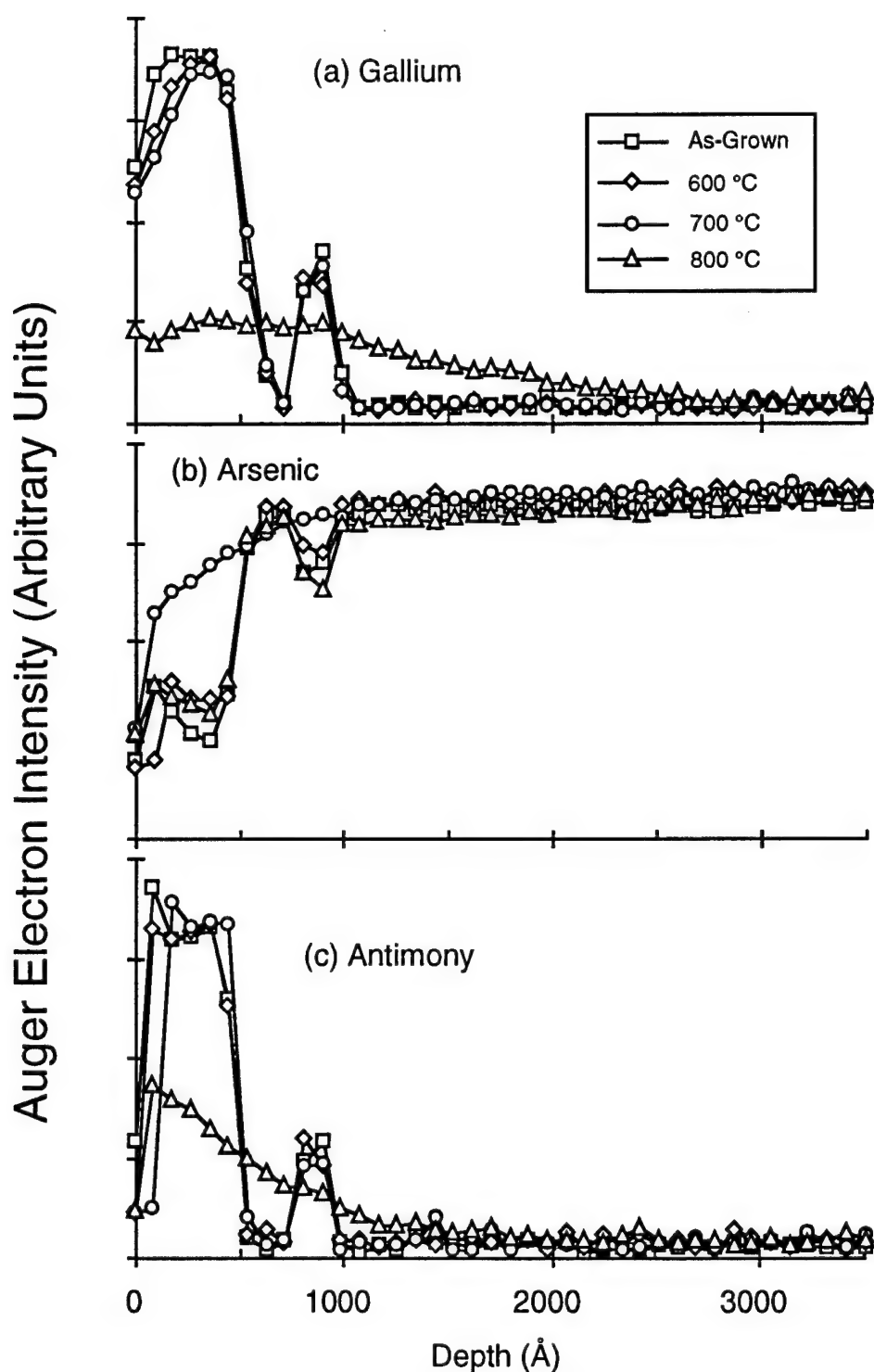


Figure 4.8. AES depth profile for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 500 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. The spectra were measured as-grown, following rapid thermal annealing for 10 seconds at 600 °C, 700 °C, and 800 °C. The (a) Ga, (b) As, and (c) Sb depth profiles are shown.

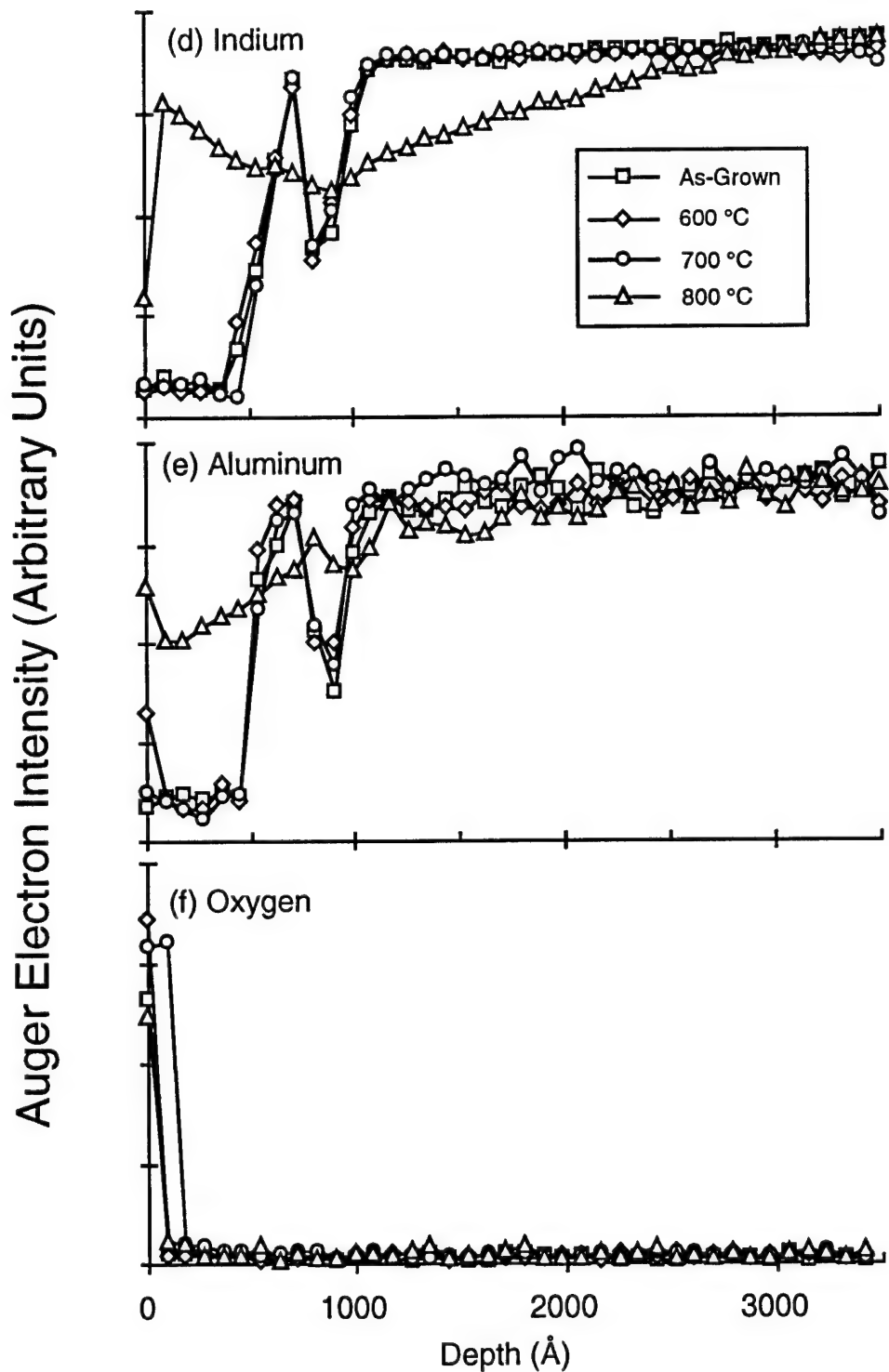


Figure 4.8(cont.). AES depth profile for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 500 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer. The spectra were measured as-grown, following rapid thermal annealing for 10 seconds at 600 °C, 700 °C, and 800 °C. The (d) In, (e) Al, and (f) O depth profiles are shown.

4.3 Temperature Dependence of the Direct Band Gap Energy and Donor-Acceptor Transition Energies in p-GaAsSb*

Optical characterization of epitaxially grown layers has allowed optimization of growth conditions for GaAs_{1-x}Sb_x produced by organometallic vapor phase epitaxy (OMVPE) [10] and molecular beam epitaxy (MBE) [11-14]. A single emission peak was previously observed in the photoluminescence (PL) spectra of undoped GaAs_{1-x}Sb_x at temperatures of 77 K [10], 4 K [11,12], and 2 K [13] when Sb compositions at or near the lattice matched condition were used ($0.45 \leq x \leq 0.55$). This PL emission peak was attributed to nonexcitonic, residual impurities of an unspecified nature. The peak position was observed to shift to higher energies with increasing excitation intensity [12]. A lower intensity, secondary peak located approximately 30 meV below the large peak was noted at $T = 4$ K [12] and 2 K [14]. In these studies, neither of the two peaks were tracked with respect to both temperature and optical excitation intensity at the lattice matched composition. Optical absorption spectroscopy was also used to measure E_g for $T = 300$ K [12] and 13 K [14]. However, the temperature dependence of E_g was not reported for lattice matched epilayers.

This section reports the existence of two emission peaks in Be-doped, lattice matched GaAs_{0.51}Sb_{0.49}. The emission peaks were studied as a function of temperature and excitation intensity (I_{ex}) using photoluminescence. Optical absorption results were used to determine E_g as a function of temperature and to obtain the Varshni coefficients α and β .

4.3.1 Experimental Approach. GaAs_{1-x}Sb_x samples were grown by MBE on semi-insulating, Fe-doped, (100)-oriented InP substrates. The GaAs_{1-x}Sb_x layer was 3 μm thick with a Be concentration of $N_A = 1 \times 10^{17} \text{ cm}^{-3}$ as measured by Hall effect at $T = 300$ K. A 500 °C substrate temperature with a 20 rpm rotation was used during GaAs_{1-x}Sb_x growth. The Sb composition was determined by double-crystal X-ray diffraction

* Results from this section were published in *Applied Physics Letters*, reference [9].

measurements, monitoring reflection from the (004) planes in the InP and GaAs_{1-x}Sb_x layers. Photoluminescence spectra were obtained at $2\text{ K} \leq T \leq 300\text{ K}$ by excitation of the sample with the 0.488 and 0.5145 μm lines of a multi-mode Ar laser. Emission was monitored with a 1.5 m spectrometer and a liquid N₂ cooled Ge photodetector. Optical absorption spectra were acquired using a Cary 5E spectrophotometer with a 175 - 3300 nm spectral range. A closed cycle refrigerator attachment allowed absorption measurements over a temperature range of $14\text{ K} \leq T \leq 300\text{ K}$.

4.3.2 Photoluminescence Results. The photoluminescence spectra are shown in Figures 4.9(a) and 4.9(b) for Be-doped, lattice matched, GaAs_{0.51}Sb_{0.49} measured at $T = 2\text{ K}$. Figures 4.9(a) and 4.9(b) show the large and small peak luminescence, respectively, for excitation intensities of 70 mW/cm² and 7 W/cm². The 70 mW/cm² excitation intensity yielded a large peak energy of 0.796 eV with a full-width-half-maximum linewidth of 9.7 meV. The large peak energy position is close to the values of 0.795 eV [13,15] and 0.797 eV [14] previously reported. The linewidth is smaller than a previously published value of 15 meV ($T = 2\text{ K}$) [13], and close to the minimum reported value of 7.5 meV ($T = 2\text{ K}$) [14]. The small peak is located 31 meV below the large peak. The large peak and small peak positions increased simultaneously by 2 meV as I_{ex} was increased to 7 W/cm².

Other Be-doped and nominally undoped samples were measured at a 70 mW/cm² excitation intensity at $T = 2\text{ K}$. Two Be-doped samples produced large and small PL emission peaks: 0.799 eV and 0.767 eV for $x = 0.48$, and 0.803 eV and 0.768 eV for $x = 0.47$. Two undoped samples produced only a single emission peak: 0.797 eV for $x = 0.49$ and 0.800 eV for $x = 0.48$. Double PL emission peaks were thus observed only in Be-doped samples, and a single peak observed in nominally undoped samples when $x \approx 0.49$. Therefore, the small PL peak appears Be related while the large PL peak is from the residual impurity as previously reported [10-13].

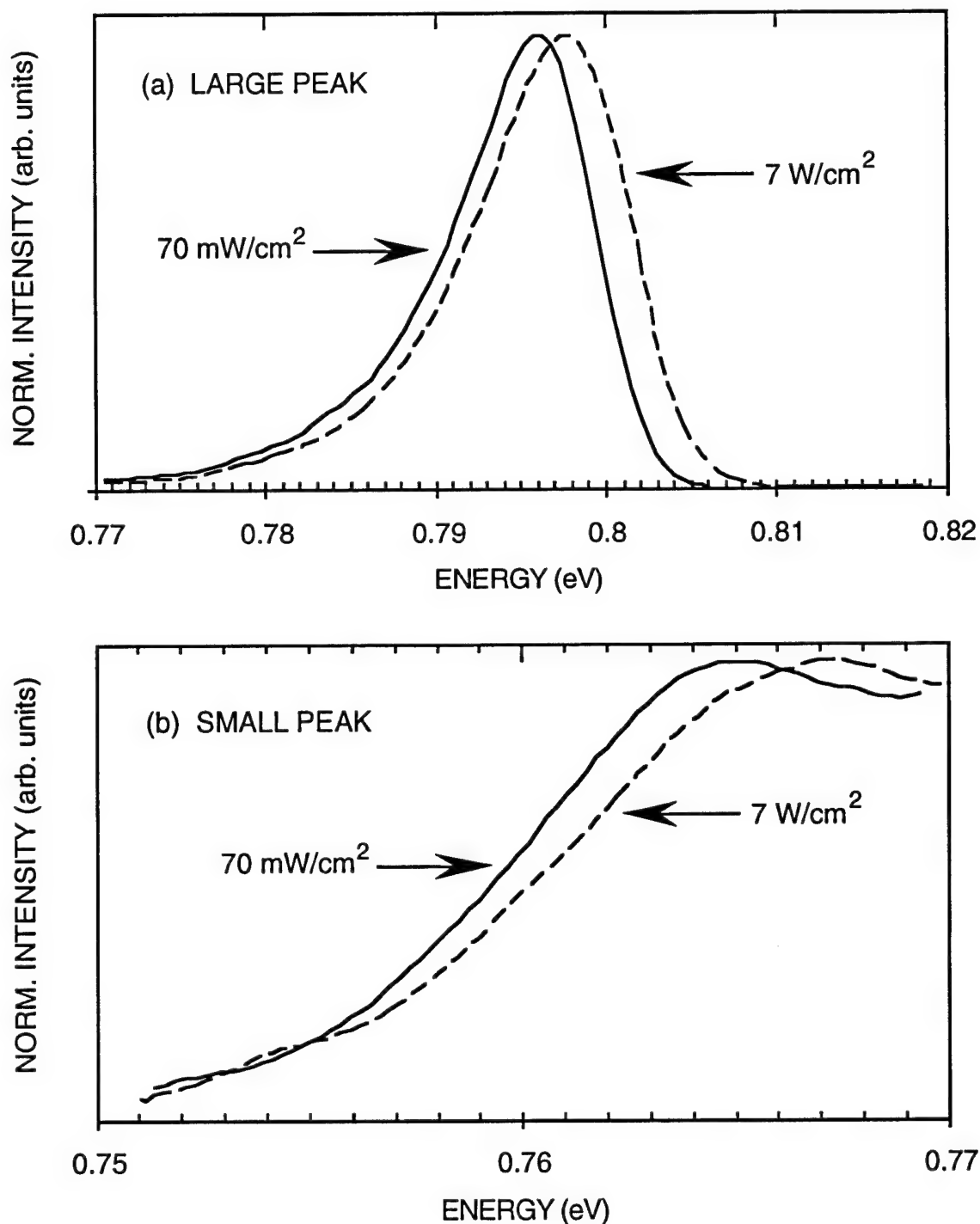


Figure 4.9. Normalized photoluminescence spectra for Be-doped GaAs_{0.51}Sb_{0.49}. The PL spectra demonstrated a (a) large peak, and (b) smaller intensity peak located 31 meV below the large peak. Both the large and small PL peaks shifted to higher energy as the excitation intensity was increased from 70 mW/cm² to 7 W/cm². The spectra were measured at T = 2 K.

A donor-acceptor (D,A) transition is evidenced by a linear relationship between the PL emission peak energy and the logarithm of I_{ex} [16]. This linear dependence is evident in both GaAs [17], GaSb [18], and other III-V semiconductors [16]. Coulombic interaction between donor and acceptor sites modifies the binding energy of the (D,A) transition. The PL emission energy for the (D,A) transition is given by [16]

$$E_{(D,A)} = E_g - E_D - E_A + \frac{q^2}{\epsilon_s} \quad (4.1)$$

where E_D and E_A are the respective ionization energies for isolated donor and acceptor impurities, q is the electron charge, ϵ_s is the static dielectric permittivity, and r is the donor-acceptor separation distance. An increase in I_{ex} causes an increase in the number of (D,A) pairs. The (D,A) pairs in close proximity increase in number faster than more distant pairs having a lower transition probability, and $E_{(D,A)}$ increases. The increase in (D,A) peak emission energy is limited by the number of (D,A) pairs on near neighbor lattice sites with the same r which are less numerous than those at distant separations.

The emission energies of the large and small peaks were measured with respect to excitation intensities between 70 mW/cm² and 7 W/cm². These results are presented in Figures 4.10(a) and 4.10(b) for GaAs_{0.51}Sb_{0.49} at temperatures of 2 K ≤ T ≤ 50 K. A linear relationship is demonstrated at each temperature using a least squares fit to the data points. The linear dependence of $E_{(D,A)}$ with respect to I_{ex} is expressed as [16,17]

$$E_{(D,A)} = E_0 \ln(I_{ex}/I_0), \quad (4.2)$$

where E_0 is the energy-shift coefficient (in meV per decade of excitation intensity) and I_0 is an arbitrary intensity reference. The small peak was no longer detected above 10 K due to linewidth broadening from the large peak. $E_{(D,A)}$ decreased in both peaks for a constant I_{ex}

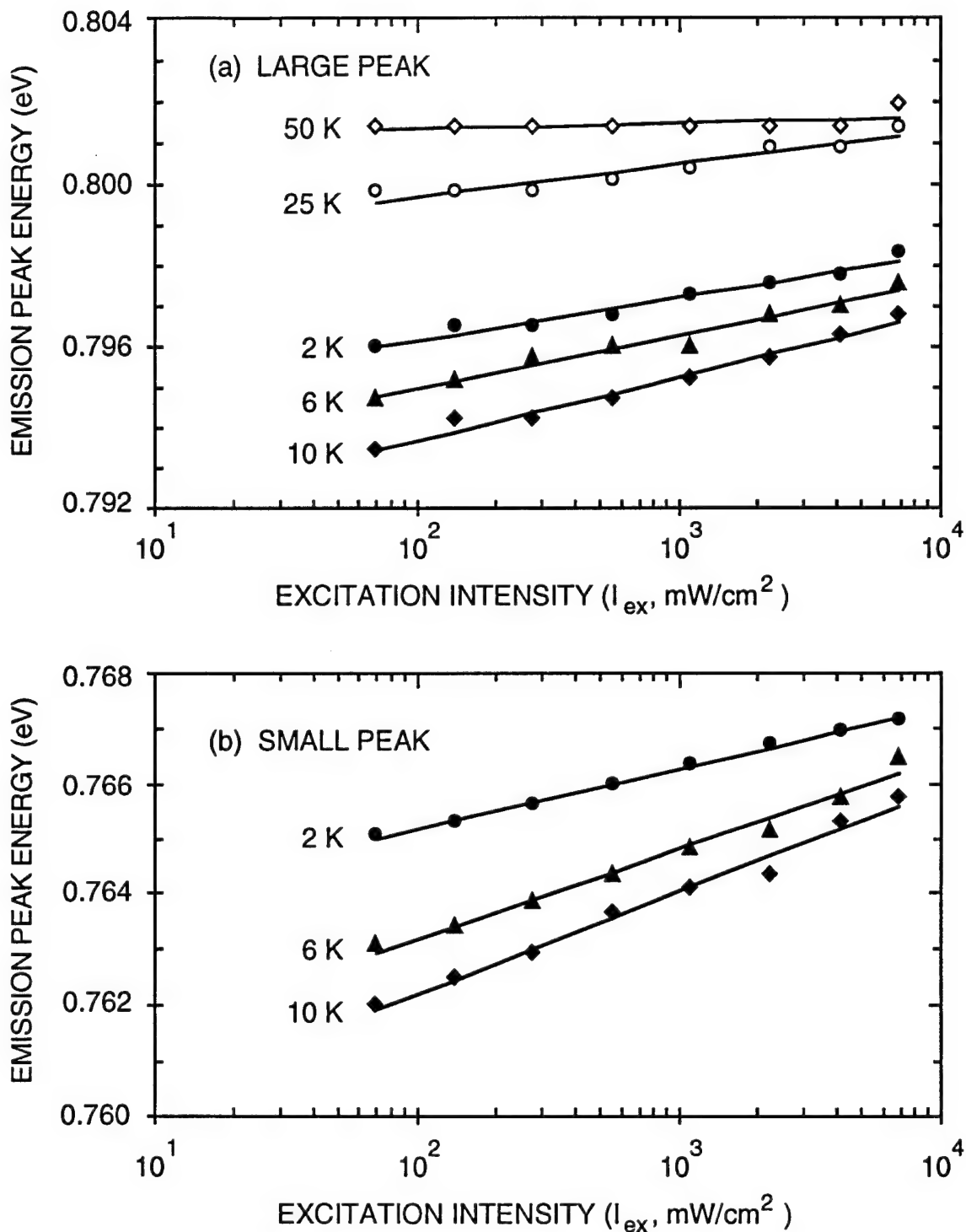


Figure 4.10. Photoluminescence peak emission energy ($E_{D,A}$) versus excitation intensity (I_{ex}) for Be-doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The PL peak positions were measured over the range $2 \text{ K} \leq T \leq 50 \text{ K}$ for (a) the large peak, and (b) $2 \text{ K} \leq T \leq 10 \text{ K}$ for the small peak. A linear relationship between the peak energy and $\log(I_{ex})$ was obtained by a least squares fit to the data at each temperature.

as the temperature was increased from 2 K to 10 K. This decrease in $E_{(D,A)}$ was previously reported due to perturbation of the conduction and valence band edges arising from an inhomogeneous distribution of the charged donor and acceptor concentrations [17]. A temperature increase permits ionized electrons to tunnel into regions of lower E_g where they recombine with nonlocalized acceptors. These nonlocalized (D,A) transitions are more probable with compositional modulation as measured in $\text{GaAs}_{1-x}\text{Sb}_x$ [19]. The large peak emission energy increased and its slope decreased at 25 K. This trend is indicative of a change towards photoemission from the free electron to acceptor level (e,A) due to increased thermalization of the residual donor level. No shift in the large peak was detected at $T > 50$ K, again implying (e,A) emission.

4.3.3 Optical Absorption Results. The direct band gap energy was measured using optical absorption. The absorption spectra of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ at 14 K and 300 K are presented in Figure 4.11. E_g was measured midway between the inflection points of the absorption edge to compensate for substrate background spectra [20]. This measurement method produced an energy difference of less than $\pm 2\%$ between E_g and the inflection points in both spectra. The measured direct energy gap at $T = 300$ K was $E_g = 0.741$ eV. This value compares closely to the calculated value of $E_g = 0.740$ eV obtained from Klem's empirical expression for $E_g(x)$ at $T = 300$ K [21]:

$$E_g(x) = 1.35x^2 - 2.05x + 1.42, \quad (4.3)$$

where x is the Sb composition, and E_g is in eV.

The direct band gap energy, and the large and small PL peak emission energies of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ are plotted as a function of temperature in Figure 4.12. A least squares fit to the E_g versus T data was made using the Varshni equation [22]

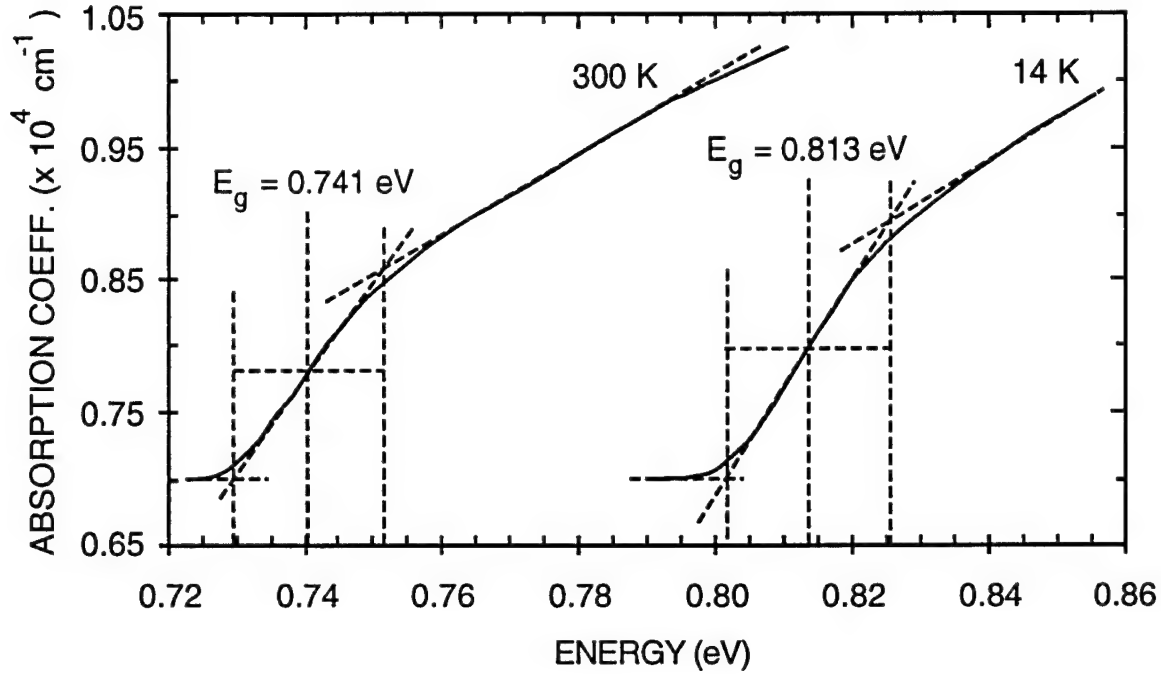


Figure 4.11. Absorption coefficient versus energy for Be-doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The absorption spectra were measured at $T = 14 \text{ K}$ and $T = 300 \text{ K}$. The direct band gap energy, E_g , is defined at the midpoint between the absorption edge inflection points as shown.

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T}, \quad (4.4)$$

providing values of $E_g(0) = 0.814 \text{ eV}$, $\alpha = 13.5 \times 10^{-4} \text{ eV/K}$, and $\beta = 135 \text{ K}$ (solid line in Figure 4.12). The large PL peak remained approximately 12 meV below E_g for temperatures $50 \text{ K} \leq T \leq 200 \text{ K}$ which is the residual acceptor ionization energy (E_A) over this temperature range assuming (e,A) transitions dominate. Presuming $E_A = 12 \text{ meV}$ at $T = 2 \text{ K}$, and using the measured values, $E_{(D,A)} = 0.798 \text{ eV}$ and $E_g = 0.814 \text{ eV}$ then $E_D = 4 \text{ meV}$. A value of $E_D = 4 \text{ meV}$ supports the concept of complete ionization of the residual donor level at $T \geq 50 \text{ K}$ since $kT = 4 \text{ meV}$ at $T = 46 \text{ K}$. Above 200 K, E_g and the large peak emission energies begin to merge, finally crossing at 300 K. This energy crossover occurs in (e,A) transitions when $E_A \leq kT/2$ [23].

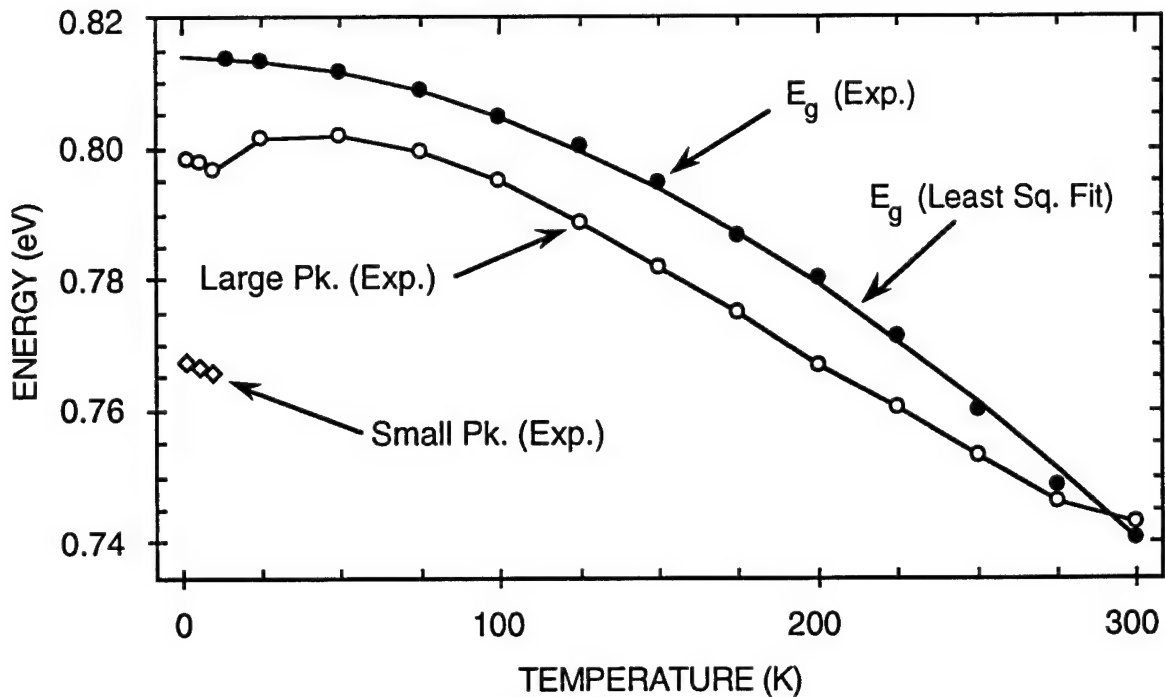


Figure 4.12. Direct band gap energy and PL emission peak energies versus temperature for Be-doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The experimental data points for E_g are closed circles. A least squares fit to the E_g data points is represented by a solid line. Experimental data points for the large PL peak are open circles connected by a solid line for clarity. Experimental data points for the small PL peak are represented by open diamonds. Above 10 K the small PL peak was no longer detectable. The PL excitation intensity was 7 W/cm^2 .

In conclusion, double emission peaks were observed in lattice matched, Be-doped GaAsSb . These two peaks exhibited (D,A) behavior when the emission peak energy was measured with respect to excitation intensity and temperature. The large (D,A) peak was due to residual impurities. The small (D,A) emission peak was observed only in Be-doped $\text{GaAs}_{1-x}\text{Sb}_x$ ($x \approx 0.49$), and indicates this transition is related to a Be acceptor. The direct band gap energy in $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ follows the same temperature relationship as other III-V semiconductors and is characterized by the Varshni equation with coefficients $\alpha = 13.5 \times 10^{-4} \text{ eV/K}$, and $\beta = 135 \text{ K}$.

4.4 Theoretical Analysis of InAlAs/GaAsSb HIGFET Characterization Results

In this section the material properties measured in Section 4.3 are used as input parameters to a one-dimensional model which produces the energy band diagram and quantized energy levels for the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET. The generated, quantized energy levels are then compared with the PL results of Section 4.2.3.

A one-dimensional, self-consistent solution to Poisson's equation and Schrödinger's equation was used to theoretically determine the quantized electron and hole energy levels in the as-grown HIGFET structure of Figure 4.1. The program is henceforth referred to as the "1D P-S program".*

In the 1D P-S modeling program, the Poisson equation

$$\frac{d^2\psi(x)}{dx^2} = \frac{-q}{\epsilon_s}(p - n + N_D - N_A + N_{DD} - N_{DA}) \quad (4.5)$$

is solved using Boltzmann statistics for the hole (p) and electron (n) concentrations. In Equation 4.5, N_{DD} and N_{DA} are the deep donor and acceptor concentrations respectively. A grid is established within each layer and Poisson's equation is solved using a finite difference method. The initial boundary condition for the Poisson equation solver is

$$q\psi(0) = \phi_{sb} \quad (4.6)$$

where ϕ_{sb} is the electron Schottky barrier height at the surface. The final boundary condition asserts maintenance of charge neutrality (zero net space charge density) at depths far below the surface

* The author of the 1D P-S program is Greg Snider of Cornell University, Department of Applied and Theoretical Physics [Reference 24]. The program is shareware and is written for the Macintosh computer.

$$\frac{d^2\psi(x=\infty)}{dx} = 0 \quad (4.7)$$

Once $\psi(x)$ is determined numerically, it is used as an input to the Schrödinger equation:

$$\left[\frac{\hbar^2}{2m_{e,h}^*} \cdot \frac{\partial^2}{\partial x^2} + V(x) \right] u_i(x) = E_i u_i(x) \quad (4.8)$$

where $u_i(x)$ is the electron/hole wave function, E_i are the energy eigenvalues, $m_{e,h}^*$ is the electron or hole effective mass and $V(x)$ is the potential energy. $V(x)$ is given by:

$$V(x) = -q\psi(x) - \Delta E_c(x) - kT \ln[n_i(0)/N_c(0)] \quad (4.9)$$

In Equation 4.9, $n_i(0)$ and $N_c(0)$ are the surface intrinsic carrier concentration, and the effective density of states in the conduction band at the surface, respectively. The direction x is parallel to the epilayer growth direction, with $x = 0$ at the surface.

The accuracy of this program was first tested by modeling single quantum wells (SQWs) in the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ system. Simulations were run using the nominal layer thicknesses and material parameters from $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and GaAs at 4 K. The quantized electron and hole energy levels for SQWs of 30, 100, and 180 Å thickness were generated. These result were compared with PL data from the $e_1\text{-}hh_1$ free exciton emission energy from two sources [25,26]. The theoretical, free exciton binding energy (E_b) for the first electron to heavy hole level ($e_1\text{-}hh_1$) [27] was added to the PL peak energy before comparing the generated and experimental energies. The percent error between the generated quantized energy levels and data from the literature was less than $\pm 0.5\%$.

Therefore, the 1D simulation program was proven accurate on the standard $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ quantum well system.

The binding energy of the $e_1\text{-}hh_1$ free exciton must be determined before comparing the 1D P-S calculated results with the PL experimental results. The $e_1\text{-}hh_1$ exciton binding energy for a 200 Å, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ SQW is small relative to the $e_1\text{-}hh_1$ transition energy ($\leq 1\%$), and less than that of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ system due to the narrower energy band gap of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ compared to GaAs [27]. The binding energy of the free exciton for the $e_1\text{-}hh_1$ transition in the $\text{InAlAs}/\text{GaAsSb}$ SQW was calculated as $E_b = 7.5$ meV [28], and found not to vary appreciably for well widths above 10 Å. Energy levels calculated by the 1D P-S program are directly comparable to the PL peak energies after subtracting E_b from the energy difference between e_1 and hh_1 .

The input material parameters required for the 1D P-S simulations are provided in Table 4.1 ($T = 4$ K). Corresponding references are listed below the table. These parameters include the 4 K values of E_g , E_D and E_A for $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ obtained by experiment in Section 4.2. Parameter ϕ_{SB} is the electron barrier height due to Fermi level pinning at the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ surface. Values of N_D and N_A are typical of those measured at $T = 4$ K in nominally undoped, semi-insulating $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and semiconducting $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ samples grown by MBE. Effective masses for $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ are calculated from the binary compound values using the actual crystal approximation [28]. In this method the alloy potential of the ternary semiconductor is approximated as the weighted average of crystal potentials for the binary compounds. The carrier masses are inversely proportional to the crystal potential. In this approximation the effective masses for the alloy $A_xB_{1-x}C$ are calculated using

$$\left(\frac{1}{m_{A_xB_{1-x}C}}\right) = x\left(\frac{1}{m_{AC}}\right) + (1-x)\left(\frac{1}{m_{BC}}\right) \quad (4.8)$$

Table 4.1. Semiconductor Material Properties Used to Calculate In_{0.52}Al_{0.48}As/
GaAs_{0.51}Sb_{0.49} HIGFET Energy Band Diagrams of Figure 4.13 (T = 4 K).

Parameter	GaAs	GaAsSb	GaSb	InAs	InAlAs	AlAs
$E_g(\text{eV})$	1.52 ^{1,9,10}	0.813 ³	0.81 ^{1,9,10}	0.418 ^{1,9,10}	1.508 ¹	2.23 ^{1,9,10}
m_e^*/m_0	0.067 ¹	0.051 ^{1,12}	0.041 ¹	0.024 ¹	0.040 ^{1,12}	0.15 ^{1,10,11}
m_{hh}^*/m_0	0.5 ¹	0.361 ^{1,12}	0.28 ¹	0.35 ¹	0.376 ^{1,12}	0.409 ¹
m_{lh}^*/m_0	0.082 ¹	0.058 ^{1,9,12}	0.045 ⁹⁻¹¹	0.026 ^{1,9,11}	0.043 ^{1,12}	0.153 ¹
ϵ_s	12.4 ¹	14.0 ^{1,10,8}	15.7 ^{1,9,10}	14.6 ⁹⁻¹¹	12.2 ^{9,1,8}	10 ^{1,10,11}
$E_D(\text{meV})$	N/A	5 ³	N/A	15 ¹	38 ^{1,8}	60 ¹
$N_D(\text{cm}^{-3})$	N/A	0	N/A	N/A	1E14 ⁶	N/A
$E_A(\text{meV})$	30 ¹	12 ^{3,7}	10 ¹	15 ¹	20	102 ¹¹
$N_A(\text{cm}^{-3})$	N/A	1E15 ⁷	N/A	N/A	0	N/A
$\Delta E_c(\text{eV})$	N/A	0	N/A	N/A	0.069 ⁵	N/A
$\phi_{SB}(\text{eV})$	N/A	N/A	N/A	N/A	0.65 ⁴	N/A

¹ "Data in Science and Technology, Semiconductors, Group IV Elements and III-V Compounds", O. Madelung (ed.), Springer-Verlag, NY, 1991.

² S. Adachi, "Materials Parameters of In_{1-x}Ga_xAs_yP_{1-y} and Related Binaries", *J. Appl. Phys.*, vol. 53, pp. 8775-8792, 1982.

³ K.G. Merkel, V.M. Bright, M.A. Marciniak, C.L.A. Cerny, and M.O. Manasreh, "Temperature Dependence of the Direct Band Gap Energy and Donor-Acceptor Transition Energies in Be-Doped GaAsSb Lattice Matched to InP", *Appl. Phys. Lett.*, vol 63, pp. 5859-5862, 1994.

⁴ C. Heedt, P. Gottwald, F. Buchali, W. Prost, H. Kunzel, and F.J. Tegude, "On the Optimization and Reliability of Ohmic and Schottky Contacts to InAlAs/InGaAs HFET", *Proc. 4th Int'l Conf. InP & Rel. Mat'ls*, pp. 238-241, 1992.

⁵ M.J. Martinez, R.L. Scherer, F.L. Schuermeier, D.K. Johnstone, C.E. Stutz, and K.R. Evans, "Measurement of the Valence Band Edge Discontinuity for the InAlAs/GaAsSb Heterojunction Lattice Matched to InP", *Proc. 4th Int'l Conf. InP & Rel. Mat'ls*, pp. 354-356, 1992.

⁶ L. Phang-Zong, "Compositionally Graded In_xAl_{1-x}As (x ≤ 0.52) Quasi-Insulator for Heterojunction Gated Field Effect Transistors", Doctoral Dissertation, Univ. Calif. - San Diego, pp. 20-32, 1991.

⁷ J.F. Klem, "Growth and Characterization of Molecular Beam Epitaxial Gallium Arsenide Antimonide and Gallium Arsenide Antimonide/Gallium Arsenide Superlattices", Doctoral Dissertation, Univ. of Illinois, p. 61, 1987.

⁸ Linear interpolation between binary semiconductor endpoint values.

⁹ D.C. Reynolds and T.C. Collins, "Excitons, Their Properties and Uses", Academic Press, NY, p. 271, 1981.

¹⁰ H.C. Casey and M.B. Panish, "Heterostructure Lasers, Part B", Academic Press, 1978.

¹¹ S. Adachi, "GaAs, AlAs, $\text{Al}_x\text{Ga}_{1-x}\text{As}$: Materials Parameters For Use in Research and Device Applications", *J. Appl. Phys.*, vol. 58, pp. R1 - R29, 1985.

¹² Actual crystal approximation.

In Table 4.1, AC represents InAs or GaSb, and BC represents AlAs or GaAs.

The results of the 1D analysis are illustrated in Figure 4.13. The simulation included the gate, channel and buffer layers of the HIGFET structure in Figure 4.1. The reader is reminded that the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer was removed for both cap layer types by wet chemical etching prior to the PL measurements. Therefore, the post-etched HIGFET structures are nominally the same - a SQW of 200 Å thickness. In Figure 4.13(a) the conduction and valence bands are shown. The Fermi level is at $E = 0$ eV. The energy band diagram shows a flat band condition across the layers due to the low doping and surface Fermi level pinning. The Fermi level is slightly below mid gap in the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel due to residual p-type doping. The quantized energy levels are shown in Figure 4.13(b) for the electrons and 4.13(c) for the first few heavy and light holes. Two electron levels are contained in the conduction band offset region. The large valence band offset ($\cong 0.9 \Delta E_g$) permits 17 heavy hole and 7 light hole energy levels. From these quantized energy levels the e_1 - hh_1 theoretical transition energy is obtained for the 200 Å well: 0.825 eV. Subtracting $E_b = 7.5$ meV from this value, yields the theoretical free exciton emission energy for the e_1 - hh_1 transition: 0.818 eV.

Comparison of the e_1 - hh_1 theoretical free exciton transition energy (0.818 eV) with the as-grown PL transition energies of Figure 4.3 is readily accomplished. As-grown PL emission energies for the e_1 - hh_1 free exciton transition are 0.834 eV and 0.804 eV for the 500 Å and 50 Å cap layer thicknesses, respectively. Thus the measured emission energies are within ± 2.0 % of the calculated e_1 - hh_1 transition energy - an encouraging result.

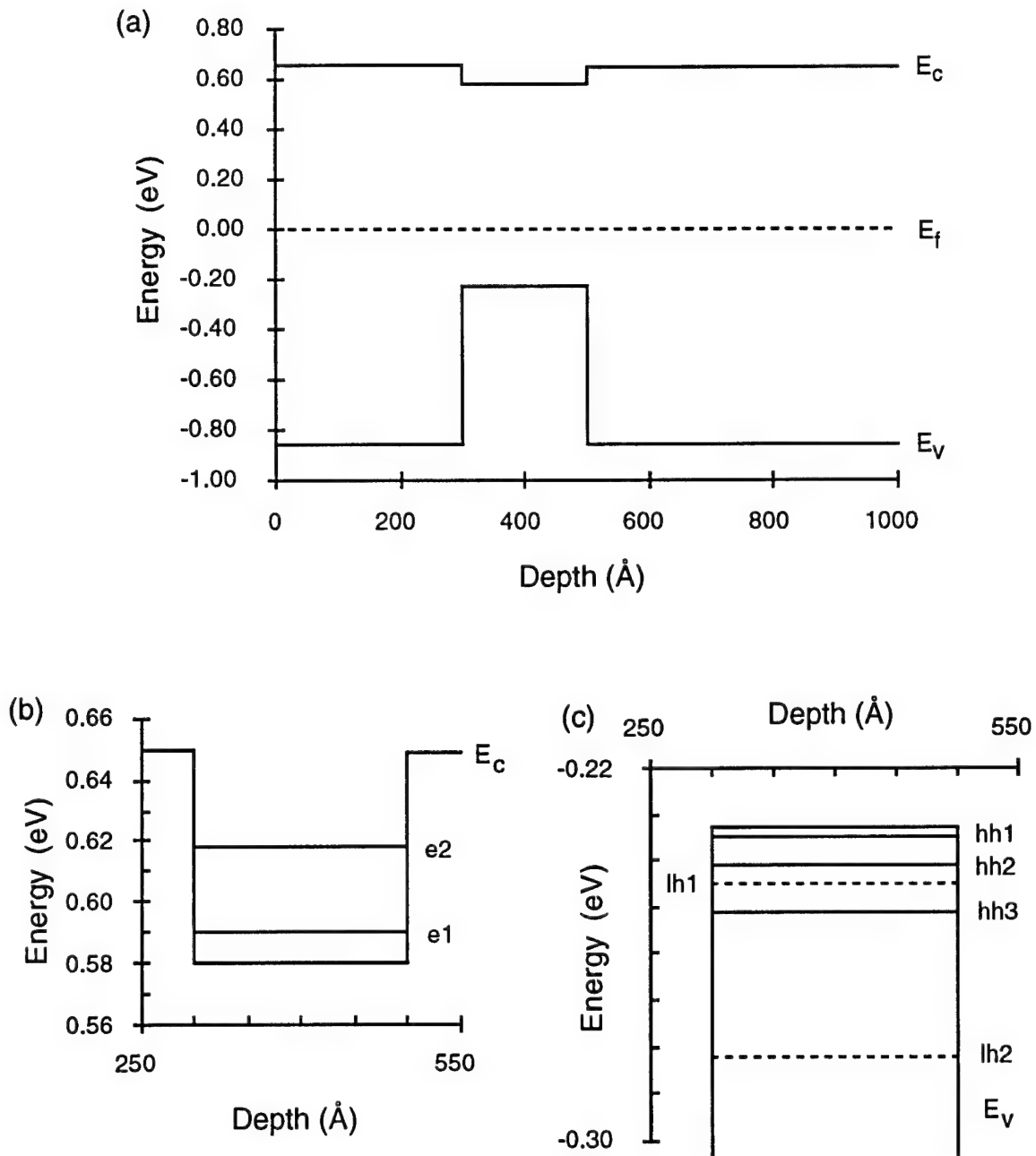


Figure 4.13. Theoretical energy band diagrams for the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET with a 200 Å channel. A 4 K temperature is simulated for comparison with the PL results of Figure 4.3. In (a) the conduction and valence bands are shown as a function of depth. The Fermi level is at $E = 0$ eV. Quantized energy levels are shown in (b) for the electrons and (c) for heavy and light holes near the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ valence band edge.

Nominally, the PL emission energies of the 500 Å and 50 Å samples should be the same since the epilayers are the same following etching of the GaAs_{0.51}Sb_{0.49} cap layer. Two effects may account for the discrepancy in the emission energies: slight variations between the two samples in the as-grown (1) channel thickness or (2) channel Sb composition. The 1-D P-S program and the SIMS and AES characterization results were employed to determine the feasibility of the two effects.

The 1D P-S program was used to determine the effect of varying the GaAs_{0.51}Sb_{0.49} channel thickness on the e_1 -hh₁ transition energy. The results of these simulations are shown in Figure 4.14. Here the e_1 -hh₁ transition energy is plotted against GaAs_{0.51}Sb_{0.49} channel thickness. The sensitivity of the e_1 -hh₁ transition energy to channel thickness is very high when the channel thickness is nominally 200 Å. A 100 Å channel thickness yields an emission energy of 0.834 eV (500 Å sample). A channel thickness greater than 500 Å is required for a PL emission energy of 0.804 eV (50 Å sample). Reflection high energy electron diffraction (RHEED) monitoring of monolayer formation during MBE growth would likely detect channel width variations greater than ± 100 Å since thickness errors of this magnitude correspond to approximately 70 monolayers in the (100) growth direction of GaAs_{0.51}Sb_{0.49}. Imprecision in channel thickness thus seems implausible due to the large variation in channel thickness required to match the measured and theoretical emission energies. The SIMS and AES also demonstrated no variation in well width thickness between the two samples, although variations on the order of 50 Å would approach the limit of depth resolution for these spectroscopies. Thus variations in well width thickness are not supported by theoretical simulation, plausible growth error, nor elemental depth profiling characterization.

Variation between the PL peak emission energies of the 500 Å and 50 Å samples is most likely a result of variation in the channel layer Sb composition. This variation was observed in the SIMS and AES spectra of Figures 4.4, 4.5, 4.7(c) and 4.8(c). A

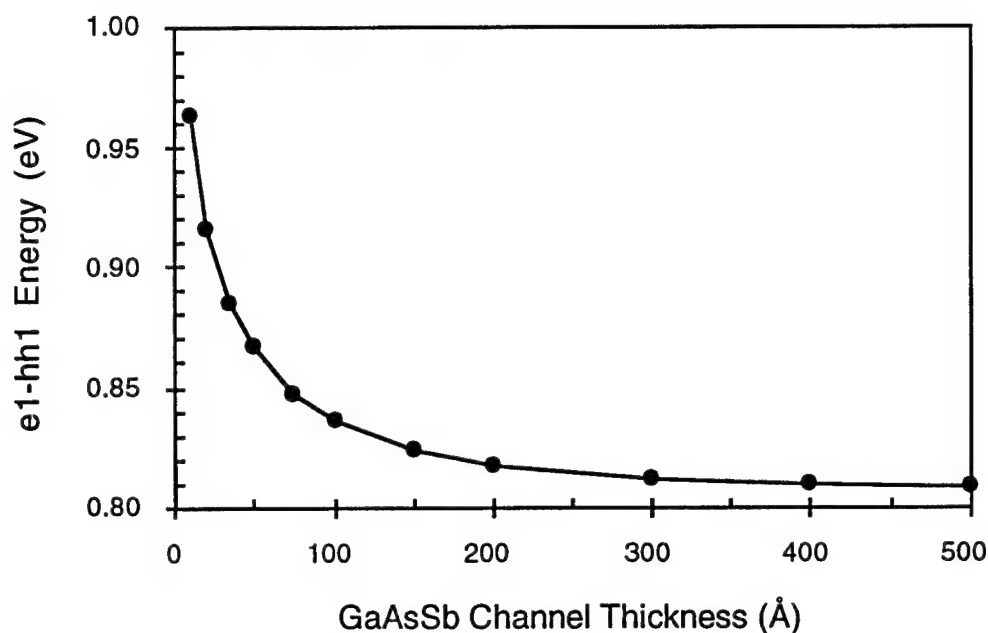


Figure 4.14. Theoretical e_1 -hh $_1$ free exciton transition energies as a function of channel thickness for the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET at $T = 4$ K.

comparison of the SIMS and AES depth profiles shows a reduced Sb content in the channel layer for the 500 Å sample. Also, the Sb content in the channel layer of the 50 Å sample is greater than its cap layer, and slightly greater than the Sb surface concentration for 500 Å sample. Reduced Sb composition would increase E_g in the channel layer and cause an increase in the e_1 -hh $_1$ free exciton transition energy in the 500 Å sample relative to the 50 Å sample.

4.5 Discussion of Results

The thermal limit of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET exhibits a definite dependence upon the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer thicknesses. Concurrence was observed in experimental results obtained from surface microscopy, photoluminescence, SIMS, and

surface and depth profiling AES. These results show SAG epilayers are intact to 600 °C. Self aligned gate epilayer degradation initiates at 700 °C and is total at 800 °C. Recessed gate epilayers are intact following annealing at 700 °C with complete corruption of the epilayers at 800 °C.

The PL results demonstrated an increase in the PL emission peak energies and linewidths as the RTA temperature was increased. The increasing linewidths of Figure 4.3(a) imply a microscopic loss of lateral homogeneity in the channel width. Loss of lateral epilayer homogeneity is evidenced by the diffusion process which occurs initially in circular regions as opposed to uniformly across the sample. The increase in peak energy (Figure 4.3(b)) indicates either a macroscopic, uniform narrowing of the heterojunction potential well width or an increase in the effective band gap of the channel layer.

Increases in PL emission energy following increased anneal temperature were previously reported in AlGaAs/GaAs [29], AlGaAs/InGaAs [30], GaAs/InGaAs [31], GaAs/GaAsSb [32] and InAlAs/InGaAs [33] quantum well structures. Between the barrier and well layers in these five systems a mismatch exists in the relative concentrations of group III elements [29-31] and group V elements [32]. Cross diffusion of elements near the well/barrier interface may produce a compositionally graded interface. A graded interface would increase the bandgap energy in the well layer near the interface and decrease the band gap energy in the barrier layer near the interface. The net result is an increase in the quantized energy levels near the bottom of the well (i.e. the e_1 energy level), and a raising of the energy levels near the top of the well. A similar situation is possible in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ system. A higher As concentration is contained in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ gate and buffer layers relative to the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel. A commensurate indiffusion of As into the channel layer with Sb outdiffusion would produce a graded layer which could raise E_g in the channel regions close the well/barrier interface.

Quantifying the exchange of barrier and channel elements is extremely difficult in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ system. In prior studies, the shift in PL emission energy was used to obtain the Al-Ga [29] and As-Sb [32] interdiffusion coefficients for AlGaAs/GaAs and GaAs/GaAsSb quantum wells, respectively. Compositional profiles were obtained using Ficke's second law, assuming a concentration independent diffusion coefficient described the interdiffusion. A study of this type is impractical for the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction due to material characterization limitations and the number of crossdiffusing elements. Prior simulation of the quantized energy levels would require, the energy gap, band edge alignments and effective masses at $T = 4\text{K}$ for $\text{In}_x\text{Al}_{1-x}\text{As}$ and $\text{GaAs}_{1-x}\text{Sb}_x$ over a range of compositions. Additional material growths, and measurements of basic $\text{In}_x\text{Al}_{1-x}\text{As}$ and $\text{GaAs}_{1-x}\text{Sb}_x$ material properties would be required. Determination of the actual compositional grading resulting from elemental cross diffusion would be difficult to determine using microstructural characterization by XRD and XTEM. The fact that the cross diffusion is not a simple exchange of two elements from a single group is a primary limiting factor to the use of a first order diffusion model. Quarternary compounds with unknown material parameters may result. Also, the cross diffusion is geometrically nonuniform as shown by the AES surface analysis of Figure 4.6.

The role of cap layer thickness in preventing epilayer degradation appears related to the ability of the elements to outdiffuse into the cap layer. Greater thermal stability of the epilayers was maintained by the RG structure to 700°C . However, deeper diffusion of some semiconductor elements was demonstrated in the RG structure at 800°C . Channel degradation in the SAG structure occurs due to outdiffusion of Ga and Sb elements toward the surface at $T \geq 700^\circ\text{C}$ as per the AES profiles of Figure 4.7. This outdiffusion is essentially the same in the circular regions at 700°C and at 800°C over the whole sample. The increase in temperature from 700°C to 800°C had little effect on the SAG diffused profiles (in contrast to the RG sample). Therefore, once outdiffusion occurs into the cap

layer, it continues until the diffusing element masses at the sample surface. Due to the thinness of the 50 Å cap layer, outdiffusing elements more readily mass at the surface at 700 °C than for the 500 Å cap layer. Outdiffusing elements in the RG sample must traverse the thicker 500 Å GaAs_{0.51}Sb_{0.49} cap layer before surface massing occurs. Thus In outdiffusion occurs from deep within the In_{0.52}Al_{0.48}As buffer layer at 800 °C in the RG sample.

4.6 Chapter IV Summary

Basic material aspects of the InAlAs/GaAsSb heterojunction and Be-doped GaAs_{0.51}Sb_{0.49} were determined. The upper thermal processing limit was determined as 600 °C for SAG and 700 °C for RG HIGFET epilayers. The HIGFET epilayer degradation is controlled by the GaAs_{0.51}Sb_{0.49} cap layer thickness. The thicker cap layer prevents initial outdiffusion of gate and buffer layer elements to the surface but allows deeper outdiffusion of these same elements as the annealing temperature is increased. Determination of both E_g and donor-acceptor impurity energy levels in GaAs_{0.51}Sb_{0.49} was accomplished using optical spectroscopy as a function of temperature for $2\text{ K} \leq T \leq 300\text{ K}$. The optical spectroscopy results of Section 4.3 were used to simulate the energy band diagrams and quantized energy levels for the In_{0.52}Al_{0.48}As/GaAs_{0.51}Sb_{0.49} HIGFET structure. The simulated results were found to agree with the experimental PL results in Section 4.1 for a 200 Å GaAsSb channel layer thickness. The results of this chapter established thermal guidelines for the design and fabrication of ohmic contacts to ion implanted regions in the In_{0.52}Al_{0.48}As/GaAs_{1-x}Sb_x HIGFET.

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V. Beryllium Ion Implantation in GaAsSb

5.1 Introduction

Achievement of a low resistance ohmic contact to the source and drain of a SAG, p-channel, HIGFET nominally requires implantation of a p-type ion species. The goals of the source/drain implant include a uniform, shallow implant profile which provides a high acceptor concentration near the surface. The implanted species must activate well upon annealing and produce a high acceptor concentration ($N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$) with little residual lattice damage. The implant anneal must also occur at temperatures which do not degrade heterojunction epilayers due to matrix element diffusion. This chapter demonstrates the sufficiency of Be ion implantation for meeting these requirements. Beryllium implantation was chosen due to: (1) it's low diffusivity relative to Zn, (2) the previous success of Be implantation in the related GaAs and GaSb semiconductors, (3) the relatively low cost and availability of commercial implantation.

In Section 5.2, a statistical representation of ion implantation is presented in order to describe Be implantation profiles with respect to depth. Simulated Be implantation profiles in $\text{GaAs}_{1-x}\text{Sb}_x$ are provided. These simulations determine nominal Be profiles prior to actual implantation. Therefore, the impact of variations in encapsulant layer thickness, implant dose and implant energy are determined *a priori*. Section 5.3 documents experimental procedures. In Section 5.4, Be implanted $\text{GaAs}_{1-x}\text{Sb}_x$ layers are characterized using optical microscopy, electrochemical profiling, SIMS and photoluminescence. The electrochemical profiling technique is highlighted with respect to measurement theory and techniques for achieving a uniform, controllable etch. In Section 5.5 the characterization results are analyzed based upon theoretical calculations of critical layer thickness for $\text{GaAs}_{1-x}\text{Sb}_x$ and Be incorporation mechanisms for GaAs.

5.2 Be Ion Implantation Theory and Simulation.

Establishing implant specifications which result in high p-type doping in GaAsSb requires foreknowledge of the resultant acceptor profile. The implant energy, dose and encapsulant layer thickness are three of the main specifications which impact the Be implantation profile. The resultant implantation profile is statistically described using the Pearson IV distribution; subsequently presented.

The Pearson IV distribution is a Gaussian distribution modified by two additional parameters (the third and fourth moments) [1]. The Pearson IV distribution is more accurate than the Gaussian distribution in describing implanted profiles away from the concentration mode [1,2]. The normalized Pearson IV distribution, $h(x)$, satisfies the following condition:

$$\int_{-\infty}^{+\infty} h(x) dx = 1. \quad (5.1)$$

where x is the depth from the GaAsSb surface.* The four moments are the range, straggle, normalized skew and normalized kurtosis which are stated in the following forms [1]:

$$\text{Range: } R_p = \int_{-\infty}^{+\infty} xh(x) dx, \quad (5.2)$$

$$\text{Straggle: } \Delta R_p = \int_{-\infty}^{+\infty} (x - R_p)^2 h(x) dx, \quad (5.3)$$

* The variable, x , is used to describe depth in this section (§5.2). This nomenclature is common in one dimensional descriptions of depth in semiconductor layers. Unfortunately, x is also commonly applied as the Sb alloy composition in $\text{GaAs}_{1-x}\text{Sb}_x$. Consequently, the x subscript is dropped in this section and “GaAs_{1-x}Sb_x” is referred to as “GaAsSb”. Specific mention of the application of x is made where an ambiguity may exist. In subsequent sections (§5.3 - §5.5), the variable d describes the depth from the GaAs_{1-x}Sb_x surface. The variable d is not used in this section since the differential sign is also d .

$$\text{Skewness: } \gamma_1 = \int_{-\infty}^{+\infty} \frac{(x - R_p)^3 h(x) dx}{\Delta R_p^3}, \text{ and} \quad (5.4)$$

$$\text{Kurtosis: } \beta = \int_{-\infty}^{+\infty} \frac{(x - R_p)^4 h(x) dx}{\Delta R_p^4}. \quad (5.5)$$

The range is the average depth of the implanted distribution. Straggle is the standard deviation of the distribution with respect to depth. Skewness is the degree of asymmetry of the depth profile. Zero skewness means the distribution is symmetric about the mode. Positive or negative skewness indicates tailing towards depths deeper or shallower than the profile mode, respectively. Kurtosis measures the degree of profile flatness near the mode. Positive kurtosis indicates the normalized implant distribution is taller and slimmer near the mode than the Gaussian normal distribution, and vice versa for a negative kurtosis. Range and straggle are typically given in angstroms, while skewness and kurtosis are dimensionless parameters.

From the four parameters of Equations 5.2 through 5.5 a set of constants are derived [1]:

$$A = 10\beta - 12\gamma_1^2 - 18, \quad (5.6)$$

$$a = b_1 = \frac{-\gamma_1 \Delta R_p (\beta + 3)}{A}, \quad (5.7)$$

$$b_0 = \frac{-\Delta R_p^2 (4\beta - 3\gamma_1^2)}{A}, \text{ and} \quad (5.8)$$

$$b_2 = \frac{-(2\beta - 3\gamma_1^2 - 6)}{A}. \quad (5.9)$$

The Pearson IV carrier concentration profile is then expressed in the following form by these constants:

$$n(x) = n_0 [b_2 x'^2 + b_1 x' + b_0]^{1/2b_2} \times \exp \left\{ \left[\frac{-(b_1/b_2 + 2a)}{(4b_2b_0 - b_1^2)^{1/2}} \right] \times \tan^{-1} \left[\frac{2b_2 x' + b_1}{(4b_2b_0 - b_1^2)^{1/2}} \right] \right\} \quad (5.10)$$

where

$$n_0 = Q_0 / \int_0^{+\infty} h(x) dx \quad (5.11) \quad \text{and} \quad x' = x - R_p. \quad (5.12)$$

The input ion dose, Q_0 , is invariably given in cm^{-2} .

A physics-based implant model produces a theoretical implant distribution once the (i) semiconductor and encapsulant layers, (ii) ion species and (iii) implantation settings (dose, energy and implant angle) are specified. A physics-based, ion implantation simulation program called POSES [3] was used in this work to obtain theoretical distribution profiles in $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ prior to actual implantation. The POSES program provides a carrier concentration profile in the following manner:

(1) The range (R_p) and straggle (ΔR_p) are computed using transport theory* and the stopping powers derived from the theory of Ziegler, Biersack and Littmark [4]. These parameters depend upon the electronic and nuclear stopping powers of the target material. The stopping powers are a function of the atomic number, mass number and atomic density of the target material.

(2) Skewness (γ_1) and kurtosis (β) are interpolated from empirical ion implantation data from GaAs. The empirical data is input from a material data file.

* As opposed to Monte Carlo theory.

(3) The four moments are inserted into the Pearson IV $n(x)$ function (Equation 5.10) and the Be implant distribution is computed.

A set of implant profiles was generated using POSES in order to optimize the Be implant dose and energy prior to implantation of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. These distributions are summarized in Figure 5.1 for a 1000 Å thick, Si_3N_4 cap layer on an infinitely thick $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layer. Implant energies of $E = 30, 40$ and 50 keV, and doses of $Q_0 = 1 \times 10^{14} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ cm}^{-2}$ were simulated. The 50 keV implant energy provided the most uniform Be concentration profile for both doses to a depth at least 500 Å below the $\text{Si}_3\text{N}_4/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ interface. The 50 keV implant energy also yielded the maximum carrier concentration for a given implant dose. According to Figure 5.1, an implant with $E = 50$ keV and $Q_0 = 1 \times 10^{14} \text{ cm}^{-2}$ provides a Be atomic concentration of $6 \times 10^{18} \text{ cm}^{-3}$ for $x \leq 500$ Å. The figure also indicates that increasing the dose to $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ should provide Be concentrations in the range $2 - 6 \times 10^{19} \text{ cm}^{-3}$ for $x \leq 500$ Å ($30 \leq E \leq 50$ keV).

These simulated results demonstrate the potential for achieving a shallow, highly-doped surface region even with an implant activation as low as 30 to 50 percent. For instance, a Be implant with $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ at 50 keV would yield a surface concentration of approximately $N_A = 2 \times 10^{19} \text{ cm}^{-3}$ assuming 30% activation. This high surface doping concentration would provide low resistance source and drain ohmic contacts to $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ based upon the theoretical specific contact resistances of Figure 2.9(b). Therefore, $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ was chosen as the maximum dose and $E = 50$ keV as a sufficient energy for the implantation experiment in the following sections.

The ability to increase dopant concentration through increased dosage is tempered by decreased electrical activation caused by increased lattice damage [5]. Increasing dosage also increases risk of lateral diffusion of the source/drain implant species during RTA of SAG devices. Consequently, final implant specifications additionally depend on the ability

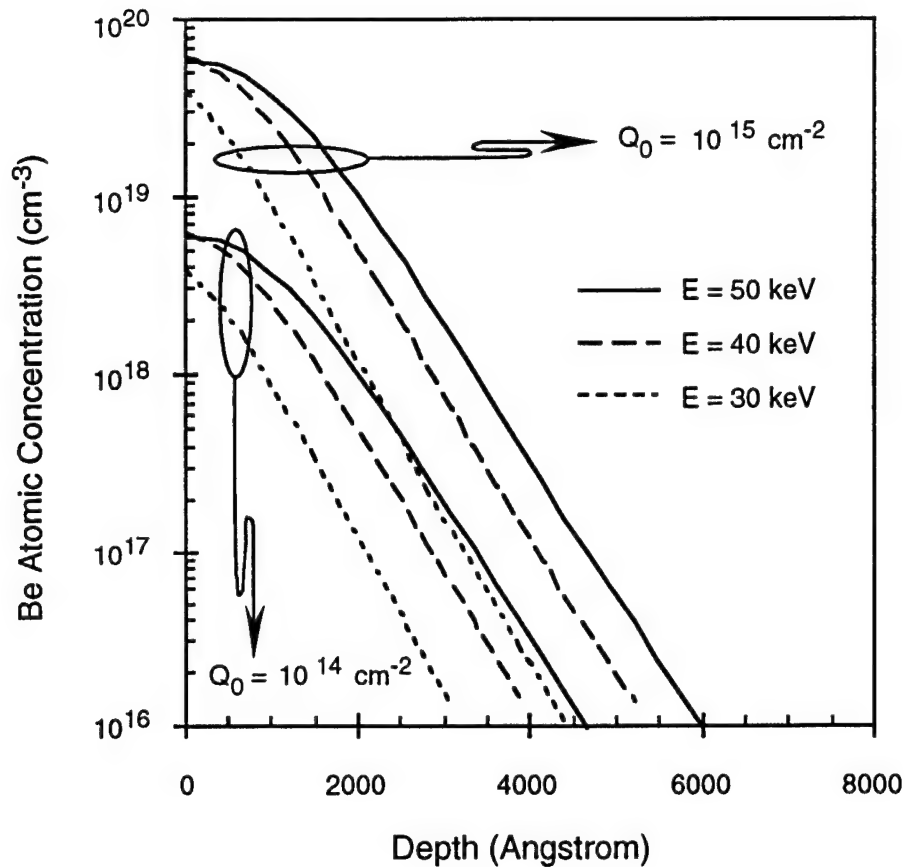


Figure 5.1. Simulated depth profiles for Be ion implantation in $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ when a 1000 Å, Si_3N_4 cap layer is used. Implant energies of $E = 30, 40$ and 50 keV, and doses of $Q_0 = 1 \times 10^{14}$ and $1 \times 10^{15} \text{ cm}^{-2}$ are shown. A depth of 0 Å corresponds to the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface.

to activate the highest carrier concentration at the lowest RTA temperature.

5.3 Sample Preparation, Implantation Parameters and RTA Conditions

$\text{GaAs}_{1-x}\text{Sb}_x$ samples were grown by MBE on (100) semi-insulating InP or GaAs substrates. Substrate growth temperature was 500°C with a rotation of 20 rpm. After growth, samples were wet chemically etched using $\text{HCl}:\text{H}_2\text{O}$ (1:10) then $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ (1:20) to stabilize the surface and reduce oxidation. A Si_3N_4 layer, nominally 1000 Å thick, was next grown by PECVD on sample surfaces at 350°C . After Si_3N_4 deposition,

samples were implanted at $E = 50$ keV, using doses of $Q_0 = 5 \times 10^{14}$ or $1 \times 10^{15} \text{ cm}^{-2}$, at $\theta = 7^\circ$ off normal. Following implantation, samples were subjected to RTA in a Heatpulse 610 system in a forming gas ambient (95 % Ar, 5% H_2) with a 10 sccm flow. Samples were enclosed in a graphite ring and covered with a GaAs wafer during RTA to limit As sublimation. The anneal time was 10 seconds in each case. RTA temperatures are subsequently described in the appropriate section. Following RTA, the Si_3N_4 was removed with a combination of O_2 and Freon 14 using reactive ion etching (RIE).

5.4 Characterization of Be Implanted GaAsSb

5.4.1 Optical Microscopy Results. Ten second anneals were initially performed at $T = 600, 700, 800$ and 900°C on $1 \mu\text{m}$ thick $\text{GaAs}_{0.51}\text{Sb}_{0.49}/\text{InP}$ samples implanted at $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$. This temperature range was selected in an attempt to maximize both implant activation and lattice reconstruction based upon results of Be implantation in GaAs [5-9]. Following annealing at 700°C , severe degradation of the Si_3N_4 layer was observed. The Si_3N_4 crystallized into floral-type patterns which flaked off when lightly scraped. Removal of the degraded Si_3N_4 was still possible by RIE in Freon 14 and O_2 . Annealing at temperatures of 800 and 900°C further degraded both the Si_3N_4 and the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. Fissures in the Si_3N_4 were observed down to the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. The $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface was rough and darkened in the fissure regions. The Si_3N_4 was hard in texture and was not removable by RIE. The reaction at 700°C , warranted further investigation of potential degradation sources at this temperature.

The reaction at 700°C was initially thought related to either: (1) the wet chemical surface preparation given the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ prior to Si_3N_4 deposition, or (2) the quality of the deposited Si_3N_4 . In order to validate the surface preparation and Si_3N_4 deposition conditions, a systematic comparison was made between Si_3N_4 deposited on $\text{GaAs}_{0.5}\text{Sb}_{0.5}$, GaAs and Si. A $3 \mu\text{m}$ layer of unimplanted $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ (grown on GaAs at a substrate

temperature of $T_{\text{subs}} = 580\text{ }^{\circ}\text{C}$) was subjected to the same surface preparation and deposition conditions previously mentioned. Also, pieces of GaAs and Si were given the same surface preparation and deposited with Si_3N_4 along side the $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ piece. All three samples were then simultaneously subjected to RTA at $700\text{ }^{\circ}\text{C}$ for 10 seconds (with a GaAs cover wafer and graphite ring). Degradation of the Si_3N_4 was again observed following $700\text{ }^{\circ}\text{C}$ RTA on the $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ piece. However, no visible change in the GaAs and Si pieces was observed after RTA. The wet chemical preparation and Si_3N_4 quality were thus validated as non-contributors to the surface reaction due to the preservation of the GaAs and Si samples. Therefore, the Si_3N_4 degradation appeared solely related to the $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ epilayer as subsequently shown in optical micrographs.

Optical micrographs of the $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ surface are shown in Figures 5.2(a) through 5.2(c). The $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ is shown as-grown, post $700\text{ }^{\circ}\text{C}$ RTA (with degraded Si_3N_4 surface), and post $700\text{ }^{\circ}\text{C}$ RTA with the Si_3N_4 removed. The as-grown surface is uniform with slight roughness. This surface roughness is indicative of $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ films grown on GaAs at $T_{\text{subs}} = 580\text{ }^{\circ}\text{C}$ [10]. The degraded Si_3N_4 surface is shown in Figure 5.2(b). This micrograph was taken from a region near the beveled edge of the MBE wafer. No $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ covers the GaAs substrate at the beveled edge. Thus the lower part of Figure 5.2(b) has a $\text{Si}_3\text{N}_4/\text{GaAs}_{0.5}\text{Sb}_{0.5}/\text{GaAs}$ layer configuration while the upper portion is only $\text{Si}_3\text{N}_4/\text{GaAs}$. Like the bulk GaAs piece, the Si_3N_4 remained intact over the GaAs edge portion of the $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ wafer. The $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ surface was slightly deteriorated following removal of the Si_3N_4 after RTA as in Figure 5.2(c). The deterioration appears as lighter regions.

The reaction between $\text{GaAs}_{1-x}\text{Sb}_x$ and Si_3N_4 established a temperature limit of $T < 700\text{ }^{\circ}\text{C}$ for single layer, lattice matched $\text{GaAs}_{1-x}\text{Sb}_x$. RTA of unimplanted $\text{GaAs}_{0.5}\text{Sb}_{0.5}/\text{GaAs}$ and $\text{GaAs}_{0.51}\text{Sb}_{0.49}/\text{InP}$ samples was next performed at $650\text{ }^{\circ}\text{C}$ in order to further bracket the maximum anneal temperature which maintained

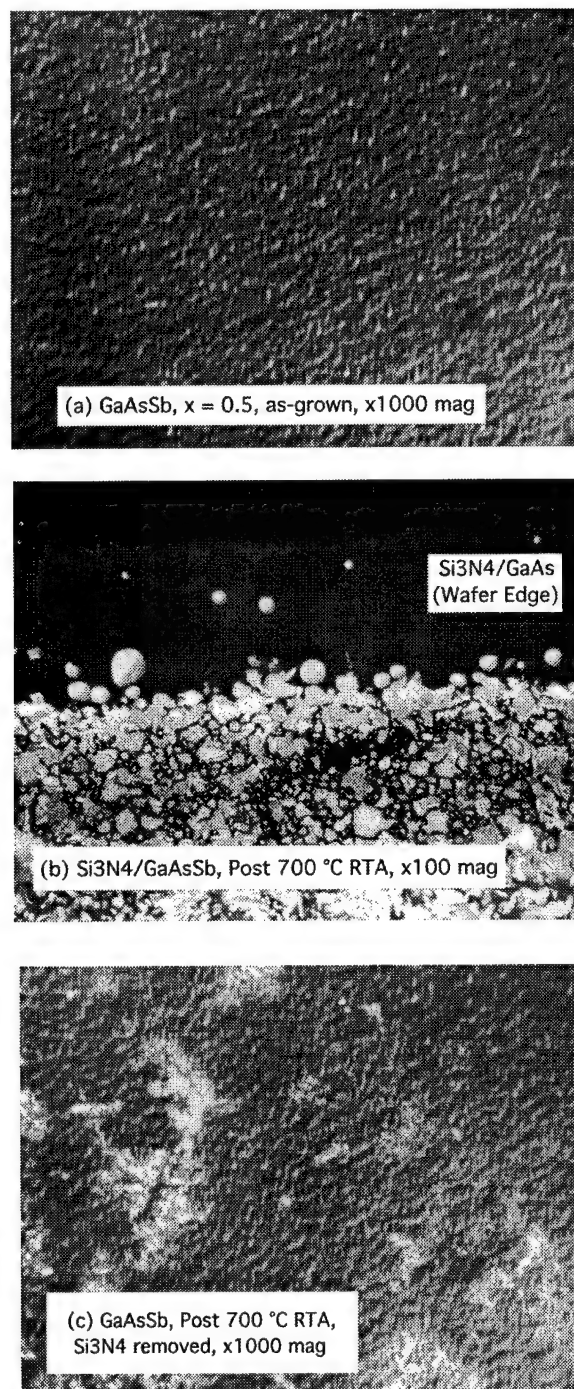


Figure 5.2 Optical micrographs of GaAs_{0.5}Sb_{0.5} sample subjected to RTA: (a) as-grown GaAs_{0.5}Sb_{0.5} surface, (b) degraded Si₃N₄ layer on top of GaAs_{0.5}Sb_{0.5} following RTA at 700 °C for 10 seconds, and (c) GaAs_{0.5}Sb_{0.5} surface following removal of the degraded Si₃N₄ layer by RIE. Si₃N₄ covering the GaAs substrate is visible at the top of the micrograph in (b) and is nondegraded.

surface integrity. The anneals performed at 650 °C used the same RTA conditions previously described. Two anneal times, 10 seconds and five minutes, were used. The longer, five minute anneal was used to bracket time effects at a temperature below 700 °C. No reaction between the $\text{GaAs}_{1-x}\text{Sb}_x$ and the Si_3N_4 was observed on either sample following the 10 second, 650 °C RTA. The Si_3N_4 was also easily removed by RIE and no degradation of the $\text{GaAs}_{1-x}\text{Sb}_x$ surface was observed. The five minute, 650 °C RTA caused degradation of the Si_3N_4 and $\text{GaAs}_{1-x}\text{Sb}_x$ only at the sample edges. The Si_3N_4 at the edges was removable by RIE. These observed effects established the necessity of performing RTA at or below 650 °C in order to prevent surface degradation.

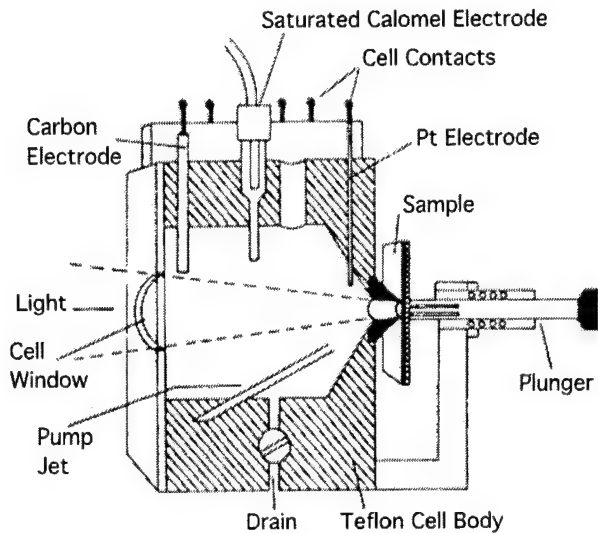
5.4.2 Electrochemical Profiling Results. Electrochemical dopant profiling was performed on Be-implanted samples using a Polaron system.* The electrochemical method is advantageous compared with other methods of implant profiling [11-14]. The electrochemical method permits profiling of activated Be ion densities without lithographic patterning as required in C-V measurements. SIMS provides Be ion profiles, including both interstitial and substitutional ions, but doesn't yield the density of activated ions. Hall effect measurements produce the sheet carrier concentrations at the sample surface (N_s in cm^{-2}). In epitaxially doped, bulk layers the Hall method yields the Be acceptor concentration simply as $N_A = N_s/t$ where t is the thickness of the bulk layer. However, in ion implanted samples a nonuniform doping contour requires successive etching and N_s measurements to obtain the acceptor density profile. Obtaining a uniform, measurable etch of small Hall samples ($4 \times 4 \text{ mm}^2$) is difficult. The electrochemical method uses smaller and more repeatable etch steps compared with the wet chemical etching procedure used in Hall measurements. Disadvantages of the electrochemical method include fairly large sample sizes (approximately 4 cm^2) and sample destruction due to etching.

* Polaron is a trade name of the Bio-Rad Corporation. Electrochemical profiling and Polaron measurement are used interchangeably henceforth.

5.4.2.1 Electrochemical Profiling System and Theory. A brief overview of the electrochemical profiling process and measurement system is warranted since the procedure is not as common as the C-V or Hall techniques. A cross-sectional view of the Polaron electrochemical cell is shown in Figure 5.3(a). The corresponding simplified circuit diagram is provided in Figure 5.3(b) [15]. A plunger maintains the semiconductor sample surface in contact with a circular sealing ring, ensuring a well defined etch area. The etch hole diameter is nominally 1 mm on the system used. The chamber is filled with an electrolytic solution of sodium hydroxide (NaOH) with ethylene diamine tetra-acetic acid (EDTA). The electrolytic solution forms a Schottky barrier at the semiconductor surface and simultaneously provides a means for controlled anodic etching [11]. The pump jet maintains a stream of fresh electrolyte at the sample surface and removes air bubbles from the semiconductor surface. Ohmic contact is made with the unetched portion of the sample surface using two wire electrodes and an In-Ga eutectic paste. Current is passed between one of the ohmic contacts and the carbon electrode while voltage is measured between the other ohmic contact and the saturated calomel electrode (SCE). Anodic etching is used to remove the epilayers. In anodic etching, an applied DC current causes a continuous oxidation-reduction reaction whereby NaOH oxidizes the semiconductor surface and EDTA removes the oxidized epilayers. N-type samples are illuminated with light in order to create holes for anodic etching. P-type samples require no illumination since holes are readily available.

Carrier concentration measurements are obtained using a capacitance-voltage model. A series resistance, R , exists between the In-Ga contacts and the semiconductor surface. A capacitance, C , represents the depletion layer capacitance at the semiconductor surface. The electrolyte-semiconductor junction is modeled as a simple RC circuit. Capacitance measurements are made between the ohmic contacts and the Pt electrode. An AC signal at four electrodes within the electrolyte is frequency modulated and the corresponding

(a)



(b)

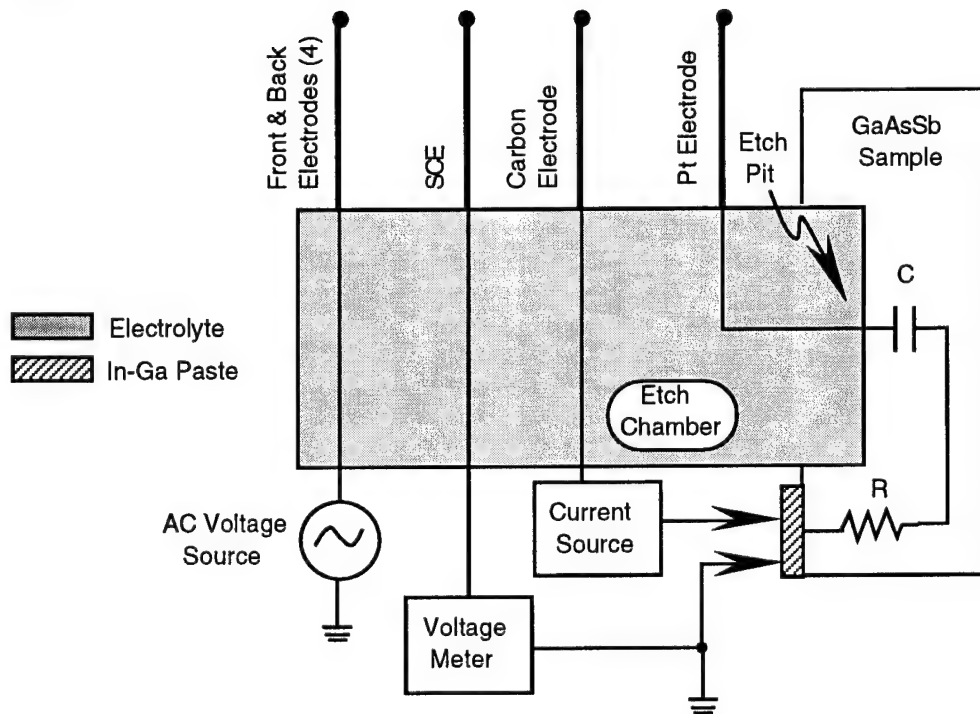


Figure 5.3. Polaron electrochemical etching cell showing (a) cut away view of the etching chamber, and (b) equivalent circuit diagram. (From Reference [15].)

change in the capacitance is measured at the Pt electrode. The Schottky formula for the depletion layer capacitance is given by [12]

$$C = \left(\frac{qN\epsilon_s}{2\psi} \right)^{1/2} A \quad (5.13)$$

where q is the electron charge, N is the net dopant concentration, ϵ_s is the semiconductor dielectric permittivity, ψ is the barrier height potential, and A is area of the etch surface. The corresponding depletion layer width is

$$W = \frac{\epsilon_s A}{C} \quad (5.14)$$

The carrier concentration between the depletion layer and the underlying field free region is then expressed as

$$N = \frac{2\epsilon_s}{q} \cdot \frac{\delta\psi}{\delta(W^2)}, \quad (5.15)$$

where $\delta\psi$ is the modulation of ψ . The etch depth is obtained from time integration of the dissolution current using Faraday's Law:

$$W_E = \frac{M}{\eta F D A} \int_{t_1}^{t_2} I \, dt, \quad (5.16)$$

where M is the molecular weight of the semiconductor, η is the number of charge carriers transferred per molecule of material dissolved, F is the Faraday (9.64×10^4 C) and D is the semiconductor density. The carrier concentration is measured at a total depth from the original semiconductor surface given by the sum of the depletion width and the etch depth:

$$d = W + W_E. \quad (5.17)$$

Thus in the Polaron process a depletion measurement is taken following each etch cycle and Equation (5.15) is plotted against Equation (5.17) to obtain $N(d)$.

Epitaxially doped GaAs_{0.5}Sb_{0.5}:Be/InP samples were measured using the Polaron system. Measurement of epitaxially doped material allows comparison of the electrochemical profiling with Hall effect characterization. The results of Polaron profiling on these GaAs_{0.5}Sb_{0.5}:Be samples are given in Figure 5.4. Both Hall measurements (single, solid points) and Polaron profiles (connected, open points) are plotted in the figure. The Polaron is limited to measuring the atomic concentration to within the depletion width of the surface. Therefore, the first acceptor concentration measurement points for the more highly doped sample were closer to the surface. Uniform doping concentrations to the 5000 Å target etch depth were exhibited by both samples. The Hall values are the carrier concentrations measured at the surface. The Hall values at the surface are within 45% of the values measured by the Polaron. This difference between the Hall and Polaron measurements are within the limits previously reported on electrochemical profiles of GaAs:Si [13].

5.4.2.2 Improving Etch Profile Uniformity. Continued electrochemical profiling of Be-implanted GaAs_{1-x}Sb_x demonstrated that improvement in the etch uniformity was needed. The process used to achieve a uniform etch is shown in Figures 5.5 through 5.10. Table 5.1 summarizes etch pit profilometry measurements corresponding to Figures 5.5 through 5.10. Simultaneous reference to the figures and table occurs during the following discussion.

An explanation of the entries in Table 5.1 is necessary before viewing the Polaron and Dektak results in Figures 5.5 through 5.10. The molar ratio of EDTA/NaOH

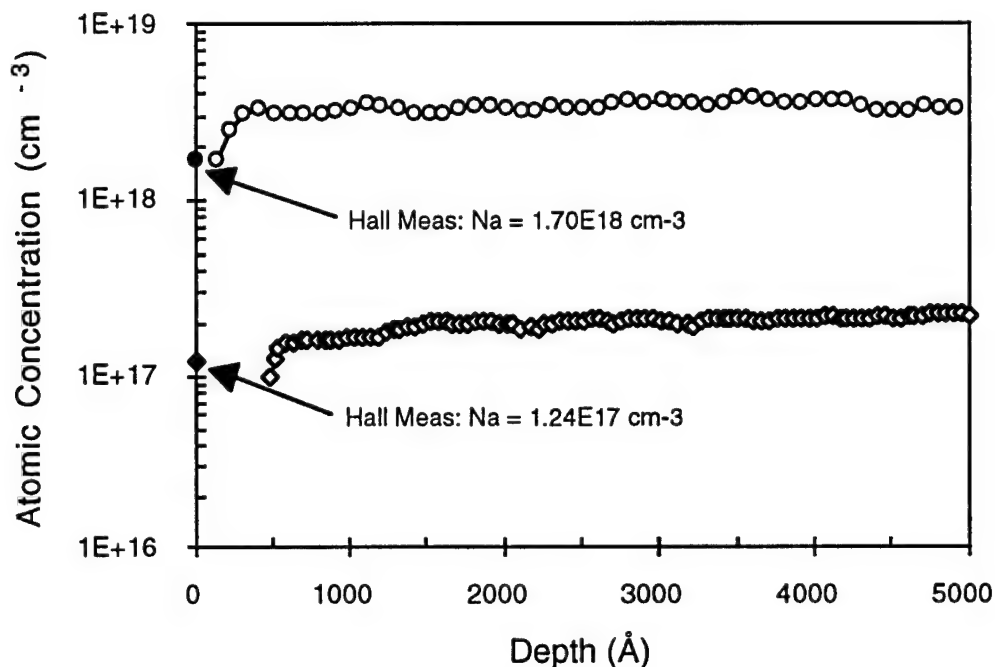


Figure 5.4. A comparison of Polaron electrochemical profiles and Hall surface measurements for two, epitaxially doped $\text{GaAs}_{0.5}\text{Sb}_{0.5}\text{:Be}$ samples grown on InP by MBE. The $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ epitaxial layers were $1\text{ }\mu\text{m}$ thick for the upper trace and $3\text{ }\mu\text{m}$ thick for the lower trace.

describes the amounts of these two chemicals added to 250 ml of de-ionized water to form the etch solution. A 0.1/0.2 M ratio of EDTA/NaOH corresponds to 9.31/2.0 grams in 250 ml of H_2O . The etchant pump frequency is the etch distance between activations of the etchant pump in the electrochemical cell. An etchant pump frequency of $500\text{ }\text{\AA}$ means the etchant was circulated following each $500\text{ }\text{\AA}$ etch. Thus the etchant is pumped after 10 etch cycles if $50\text{ }\text{\AA}$ etch steps are used. Target etch depth is the selected value of maximum etch depth input into the Polaron profiling control program. The left-to-right and bottom-to-top etch uniformity are defined in terms of Dektak measurements taken across the center of the etch pit surface. The average depth is the average value of all the depth data points measured across the etch pit. The peak-to-valley roughness is the difference between the

Table 5.1. Surface Profile Statistical Summary: Electrochemical Etching of Beryllium Implanted GaAsSb

Text Fig. No.	EDTA/NaOH Etchant Ratio (mole/mole)	Etchant Pumping Freq. (Å)	Target Etch Depth (Å)	Left-to-Right (L->R) Uniformity (Å)			Bottom-to-Top (B->T) Uniformity (Å)		
				Avg. Depth	Pk-Val Rough.	Avg. Rough.	Avg. Depth	Pk-Val Rough.	Avg. Rough.
5.5	0.1/0.2	None	5000	3830	4270	±750	3760	3620	±950
5.6	0.1/0.2	500	5000	5740	2640	±410	5580	3970	±740
5.7	0.2/0.2	500	5000	5430	2740	±520	5290	1850	±130
5.8	0.2/0.2	25	8000	8140	1170	±180	8270	1880	±266
5.9	0.1/0.2	None	5000	5350	2000	±280	5000	5040	±1140
5.10	0.2/0.2	25	8000	7670	1310	±300	7920	1220	±220

minimum and maximum depth points along the surface. The average roughness is obtained by averaging all the surface depth data points above and below the average depth value.

The Polaron profiles of Figures 5.5 through 5.8 were measured on a 1 μm thick layer of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ on semi-insulating GaAs. This sample was ion implanted with a Be dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ at $E = 50 \text{ keV}$ through a 1000 Å thick cap layer of Si_3N_4 . The wafer piece was subsequently rapid thermal annealed at 600 °C for 10 seconds. The Si_3N_4 was then removed by RIE prior to Polaron profiling. Acceptor concentration measurements were taken after each 50 Å etch step.

The Polaron profile of Figure 5.5 was measured using a 0.1/0.2 molar ratio of EDTA/NaOH. A 5000 Å target etch depth was chosen in order to encompass the majority of the implant profile indicated by the POSES simulations of Figure 5.1. The etchant was initially not pumped as a precaution against overetching. The resulting Be concentration profile is shown Figure 5.5(a). The Be profile shows a surface concentration between $2 - 3 \times 10^{19} \text{ cm}^{-3}$ with a Pearson-type roll off to a depth of 3000 Å. From 3000 Å to 5000 Å the Be concentration was level at approximately $4 \times 10^{18} \text{ cm}^{-3}$. Dektak profiles of the etch

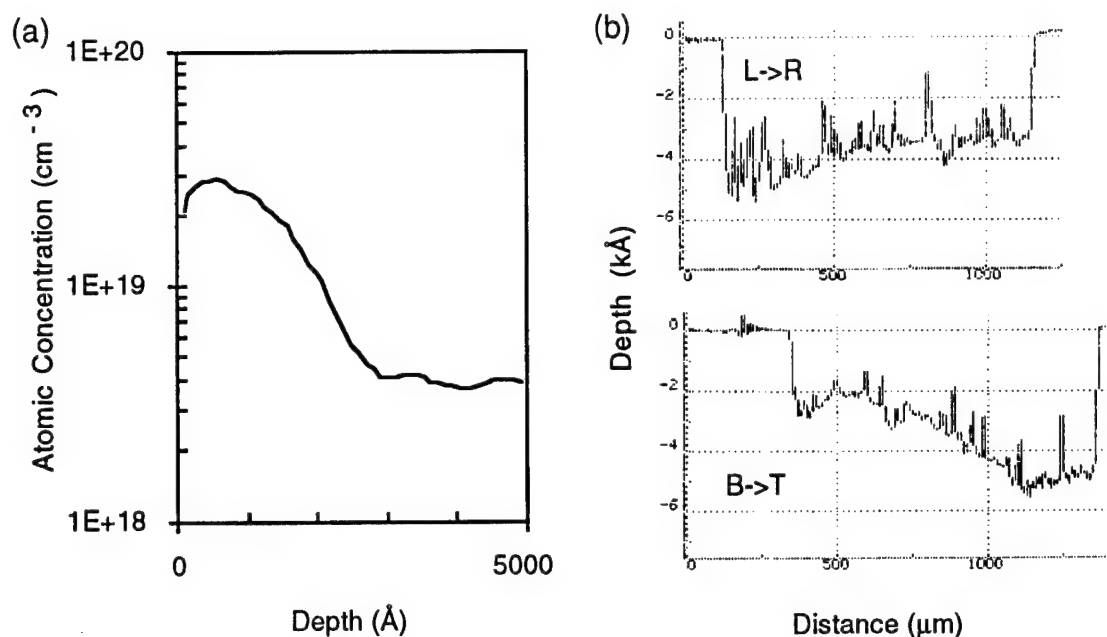


Figure 5.5. Electrochemical profiling results on Be implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ on GaAs: (a) Be concentration profile, and (b) Dektak surface profiles taken perpendicularly across the etch hole center. The Be implant and RTA conditions were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, and $T = 600^\circ \text{C}$ for 10 seconds. A 0.1/0.2 M aqueous solution of EDTA/NaOH was used with no etchant pumping.

pit are shown in Figure 5.5(b) to the right of the Be concentration plot. The upper Dektak scan was taken from left to right across the center of the etch hole (L->R) while the lower scan was obtained across the center from bottom to top (B->T). Clearly, both scans showed a rough, nonuniform etch in both directions. The etch profile had spiked protrusions with an angled, non-horizontal etch surface. Dektak statistics obtained from this surface profile are contained in the first row of Table 5.1. The entries in row one are applicable to Figure 5.5(b). Both scan directions showed an average depth approximately 1200 \AA less than the 5000 \AA target depth with a pk-val roughness $\leq 4300 \text{ \AA}$ and an average roughness $\leq 950 \text{ \AA}$. Therefore, the 0.1/0.2 EDTA/NaOH molar ratio without etchant pumping produced an underetched surface profile with a pk-val roughness on the order of the target depth and an average roughness between 15 to 19 % of the target depth. The

flattened Be profile at 3000 Å depth was considered caused by the slower etching at the bottom of the etch hole, yielding an increased value of Be concentration. Slow etching was believed caused by an inability to remove settled etch residues from the bottom wall of the etch hole. The next approach was periodic circulation of the etchant in an attempt to remove these residues without overetching.

The same electrochemical etch conditions were used to obtain Figure 5.6 except the etchant was pumped every 500 Å. The Be concentration profile near the surface was essentially the same as in Figure 5.5(a). The Be profile began to level again at depths below 3000 Å. However, the value of N_A was reduced to between $1 \times 10^{18} \text{ cm}^{-3}$ and $2 \times 10^{18} \text{ cm}^{-3}$ over the flattened profile region. The Dektak profiles showed a smoother etch in both the L->R and B->T directions. The etch along the L->R line was also flatter when compared with the previous, unpumped case. The tabulated results show overetching with average etch depths closer to the target depth than in the unpumped case (within $\pm 740 \text{ Å}$). The flatter L->R etch is verified by a reduction in the pk-val roughness from 4270 Å to 2640 Å. The pk-val roughness of the B->T etch increased very slightly. The average roughness decreased in both measurement directions and was between $\pm 8 \%$ and $\pm 15 \%$ of the target depth. Thus circulating the etchant after removing 500 Å $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ produced a smoother and overall more level etch surface but did not prevent the slower etching along the B->T line. Slower removal of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ from the bottom wall of the etch hole was thought compounded by both the angle of the incoming etchant stream and the ability to refresh the etchant. The pump hose is in a fixed position at the bottom of the electrochemical cell and points upward towards the etch hole. Consequently, during pumping, the etchant stream impinges first on the top wall of the etch hole and then circulates to the bottom wall. Repositioning of the pump hose is a delicate procedure due to risk of breakage. Hence, other methods of leveling the etch surface were attempted first.

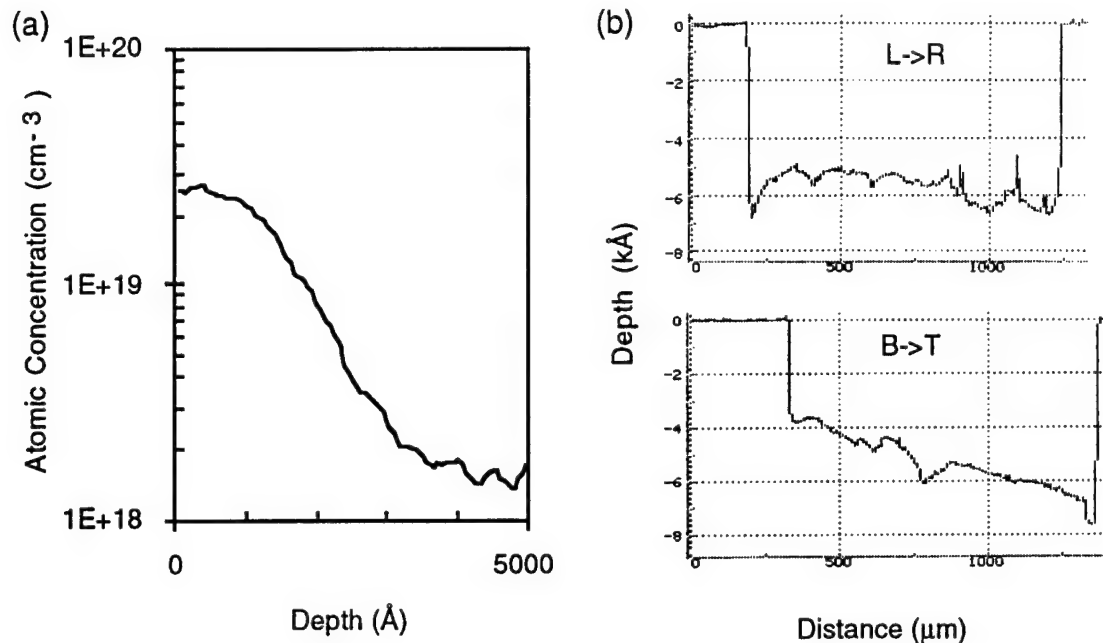


Figure 5.6. Electrochemical profiling results on Be implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ on GaAs: (a) Be concentration profile, and (b) Dektak surface profiles taken perpendicularly across the etch hole center. The Be implant and RTA conditions were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, and $T = 600^\circ \text{C}$ for 10 seconds. A 0.1/0.2 M aqueous solution of EDTA/NaOH was used with an etchant pump cycle every 500 Å.

The EDTA/NaOH molar ratio was next raised to 0.2/0.2. The acidic portion of the etchant was increased in order to speed removal of oxides on the initial etch surface and increase the etch rate in order to even out the B->T etch. Figure 5.7 demonstrates the Be concentration and surface etch profiles produced by increasing the EDTA concentration and using an etchant pump frequency of 500 Å. The resulting Be profile was similar to Figure 5.6(a) in terms of the surface and peak concentrations above $d = 3000 \text{ Å}$, and leveling at depths below 3000 Å. Considerable improvement in the overall smoothness of the etch surface was measured in the Dektak profiles. The surface along the B->T direction was essentially flat over 90 % of the etch pit with a sharp dip near the top etch wall. The L->R etch was less level when compared to the 0.1/0.2 molar ratio results of Figure 5.6(b). This fact was manifested as a slight increase in the measured pk-val and average roughness

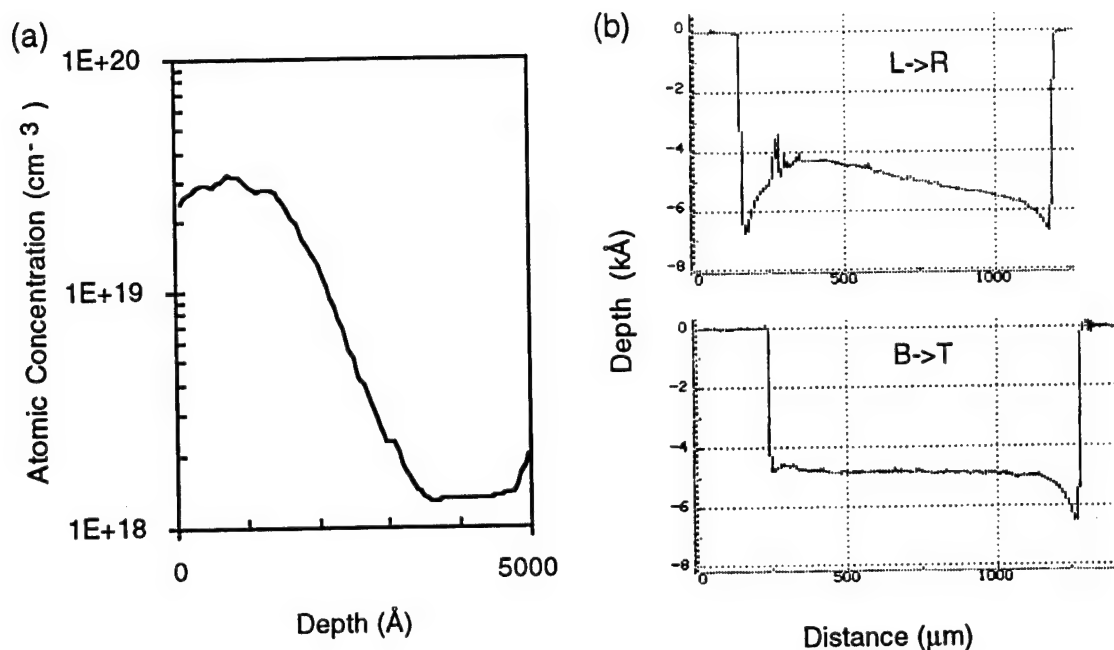


Figure 5.7. Electrochemical profiling results on Be implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ on GaAs: (a) Be concentration profile, and (b) Dektak surface profiles taken perpendicularly across the etch hole center. The Be implant and RTA conditions were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, and $T = 600^\circ\text{C}$ for 10 seconds. A 0.2/0.2 M aqueous solution of EDTA/NaOH was used with an etchant pump cycle every 500 Å.

measured for the L->R direction. The reason for the change in the L->R Dektak profile is unknown at this time. Two encouraging results emerged from this etch step. First, overetching was reduced to less than 430 Å in both profiling directions as demonstrated by the average depth. Second, the increased EDTA concentration caused deeper etching along the circumference of the etch hole. Thus the peak of the etch surface no longer occurred along the circumference but was displaced more towards the center of the etch hole. This displacement was advantageous from the standpoint of exposing the slower etching region to the circulating etchant. The overall improvement in etch uniformity to depths greater than 3000 Å indicated that the Be profile ledge at 3000 Å was real and not a consequence of etch nonuniformity.

The etchant pump frequency was increased in an attempt to take advantage of the lateral shift of the etch surface maximum height towards the hole center. However, the increase in pump frequency raised the etch current density from approximately 1.5 A/cm² to 4 A/cm² and overetching beyond the target depth occurred. A series of Polaron profiles were attempted (not shown) in which the etch voltage was varied in order to maintain the etch current density around 1.5 A/cm² as the etchant pump frequency was increased. A pumping frequency of 25 Å (two etchant circulations per application of etch current) produced the most uniform etch to a target depth of 5000 Å. The target etch depth was increased to 8000 Å after the uniform etch was obtained across the entire etch hole to a depth of 5000 Å.

Polaron and Dektak profiles in Figure 5.8 were acquired by electrochemically etching to a target depth of 8000 Å using a pump frequency of 25 Å. The uniformity of the entire etch area demonstrated that the Be concentration ledge at 3000 Å was indeed real. The Be profile ledge dropped off at approximately 6500 Å until a final acceptor density of $N_A \leq 1 \times 10^{17} \text{ cm}^{-3}$ was measured at a depth of 8000 Å. The accuracy of the Be concentration profile depth was verified by the Dektak profiles which showed improved flatness to a depth of 8000 Å. A small overetch of 140 Å (L->R) and 270 Å (B->T) was measured in the average etch depths (corresponding to overshoots of the target etch depth by 1.8 % and 3.4 % respectively). The L->R pk-val roughness and average roughness were likewise greatly improved by circulating the etchant every 25 Å versus every 500 Å. The B->T average roughness increased due to a small amount of overetching along the bottom and top walls of the etch hole. Overetching along the etch hole circumference may be unavoidable due to current crowding when the 1 µm GaAs_{0.51}Sb_{0.49} layer is etched close to the substrate. The fact that the average roughness is below ±4 % of the target etch depth in both directions is encouraging. This average roughness is better than the 5% to 10% previously reported for Polaron profiling on GaAs samples [14].

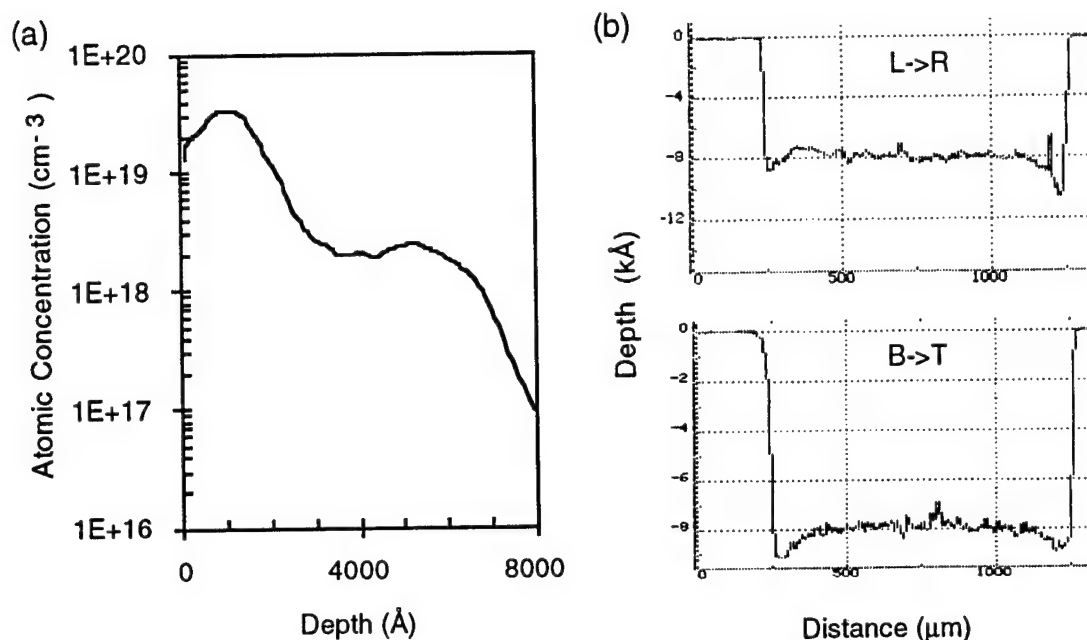


Figure 5.8. Electrochemical profiling results on Be implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ on GaAs: (a) Be concentration profile, and (b) Dektak surface profiles taken perpendicularly across the etch hole center. The Be implant and RTA conditions were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, and $T = 600^\circ \text{C}$ for 10 seconds. A 0.2/0.2 M aqueous etchant solution of EDTA/NaOH was used with a pump cycle every 25 Å.

The etch conditions were used to profile a 1 μm thick epilayer of $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ on semi-insulating InP. This sample was ion implanted with a Be dose of $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ at $E = 50 \text{ keV}$ through a 1000 Å thick cap layer of Si_3N_4 . RTA occurred at 600°C for 10 seconds. The nonoptimized etch process was first applied. The results, given in Figure 5.9, compare closely with Figure 5.5. Here profiling was implemented with a 0.1/0.2 molar ratio of EDTA/NaOH, and no etchant pumping. The Be profile had nearly the same surface concentration as the profiles in Figures 5.5 through 5.8. The profile mode was close to the same depth with a slightly higher concentration at the peak (roughly $4 \times 10^{19} \text{ cm}^{-3}$). The Be concentration continuously decreased for depths below the peak depth to a minimum value of $N_A = 2 \times 10^{16} \text{ cm}^{-3}$ at the target depth of 5000 Å. No distinct profile ledge was observed as occurred in Figures 5.5 through 5.8. Rough, nonuniform

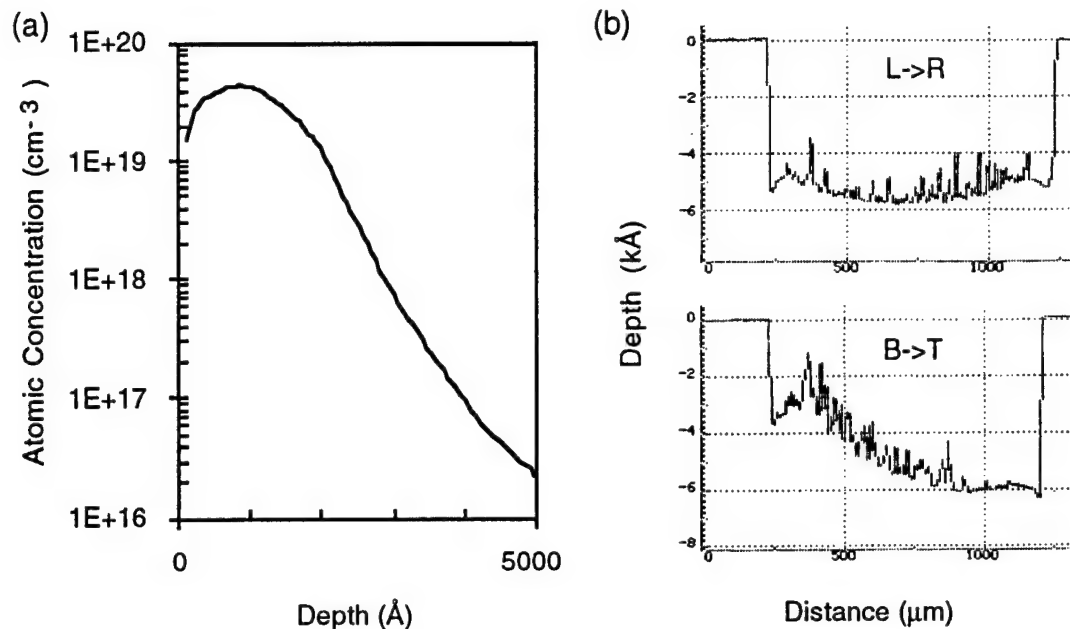


Figure 5.9 Electrochemical profiling results on Be implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ on InP: (a) Be concentration profile, and (b) Dektak surface profiles taken perpendicularly across the etch hole center. The Be implant and RTA conditions were $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, and $T = 600^\circ \text{C}$ for 10 seconds. A 0.1/0.2 M aqueous solution of EDTA/NaOH was used with no etchant pumping.

Dektak profiles were exhibited in both the L->R and B->T directions. A sloping etch surface from bottom to top was again observed as per Figure 5.5(b).

A result similar to that of Figure 5.8 was obtained on the $\text{GaAs}_{0.53}\text{Sb}_{0.47}/\text{InP}$ sample using the optimized etch conditions (0.2/0.2 EDTA/NaOH molar ratio and pump frequency of 25 \AA). These results are shown in Figure 5.10. Considerable improvement in the etch smoothness and uniformity was again realized, enabling reliable etching to depths near 8000 \AA . A distinct increase in the slope of the Be concentration profile was again demonstrated at a depth of 3000 \AA . The slight underetching in both Dektak profiling directions was within 320 \AA (4 %) of the target depth. The pk-val roughness is lower than that obtained in Figure 5.8. The average roughness is also less than $\pm 300 \text{ \AA}$ ($\pm 4 \%$) for both directions.

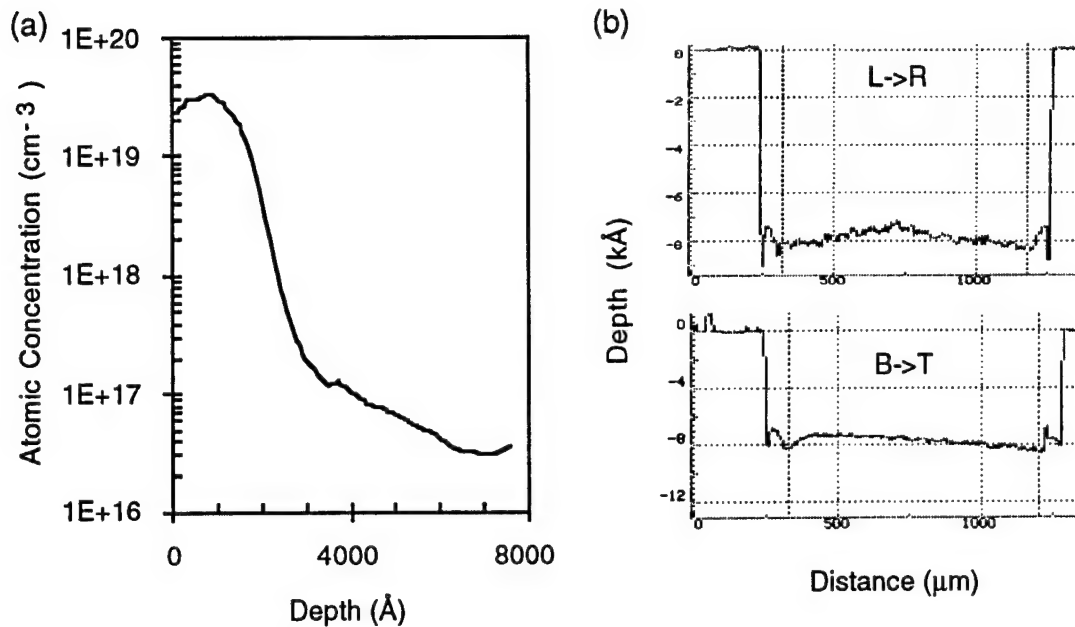


Figure 5.10. Electrochemical profiling results on Be implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ on InP: (a) Be concentration profile, and (b) Dektak surface profiles taken perpendicularly across the etch hole center. The Be implant and RTA conditions were $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, and $T = 600^\circ\text{C}$ for 10 seconds. A 0.2/0.2 M aqueous solution of EDTA/NaOH was used with an etchant pump cycle every 25 Å.

A couple of conclusions are apparent from Table 5.1 and Figures 5.5 through 5.10. First, the ability to obtain a uniform etch profile is a complex mixture of etchant molar ratio, etchant refreshment frequency and etch current. Once a satisfactory combination of these factors is obtained, constant monitoring is still dictated. Second, the use of GaAs versus InP substrates does not effect etch uniformity to depths of 8000 Å. Variations in the etchant ratio and pumping frequency produce smooth, uniform etch profiles for 1 μm $\text{GaAs}_{1-x}\text{Sb}_x$ layers on either substrate type. Third, an increase in the slope of the Be concentration profile is observed for implant doses of $Q_0 = 5 \times 10^{14}$ and $1 \times 10^{15} \text{ cm}^{-2}$ annealed at 600 °C. This increase in the slope occurs at approximately 3000 Å for both samples. The increase in slope was more severe for samples grown on GaAs with the Be profile actually plateauing.

5.4.2.3 Polaron Profiles for Be Implanted GaAsSb. Establishment of a uniform, reproducible etch process was necessary to ensure accurate representation of the Be distribution profile. The optimized etch conditions were subsequently used to determine the Be distribution in samples subjected to varying implant dosage and RTA temperature. Samples had a 1 μm thick $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ layer on an InP substrate (with a 1000 \AA Si_3N_4 cap layer). The implant doses were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ cm}^{-2}$ at 7° off normal with an energy of $E = 50 \text{ keV}$. The RTA temperatures were $T = 600$ or 650°C . This combination of parameters was chosen based upon the theoretical distributions of Figure 5.1 and the $T = 700^\circ\text{C}$ thermal limit for the Si_3N_4 degradation established previously.

Figure 5.11 shows two representative Polaron profiles for samples with $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, subjected to RTA at temperatures of 600°C and 650°C . Similarities exist in the two profiles. The mode depths were $d \approx 800 \text{ \AA}$ at both temperatures. The same Pearson-type roll off was exhibited from 2000 \AA to 4000 \AA depth. Both profiles showed non-Pearson tailing of the Be distributions for depths greater than 3000 \AA . The surface concentration in both cases was $N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$. Differences in the profiles also existed. On some of the samples a peak was observed at the surface while in others the concentration increased initially for depths proceeding from the surface. The tailing profile was not explicitly dependent upon the anneal temperature in the samples - the higher RTA temperature did not always produce a larger amount of tailing.

Representative Polaron profiles for samples with $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ are shown in Figure 5.12 for RTA temperatures of 600°C and 650°C . The surface concentration was $N_A \approx 2 \times 10^{19} \text{ cm}^{-3}$ for both of the RTA temperatures. The activated Be concentration was $N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$ from the surface to a depth of 1500 \AA . The roll off in the implantation profile was the same for both temperatures between 2000 \AA and 3000 \AA depth with a decrease in the profile slope beginning at 3000 \AA . Increasing the anneal temperature to 650°C caused the profile to flatten near the surface and tail deeper into the $\text{GaAs}_{0.53}\text{Sb}_{0.47}$.

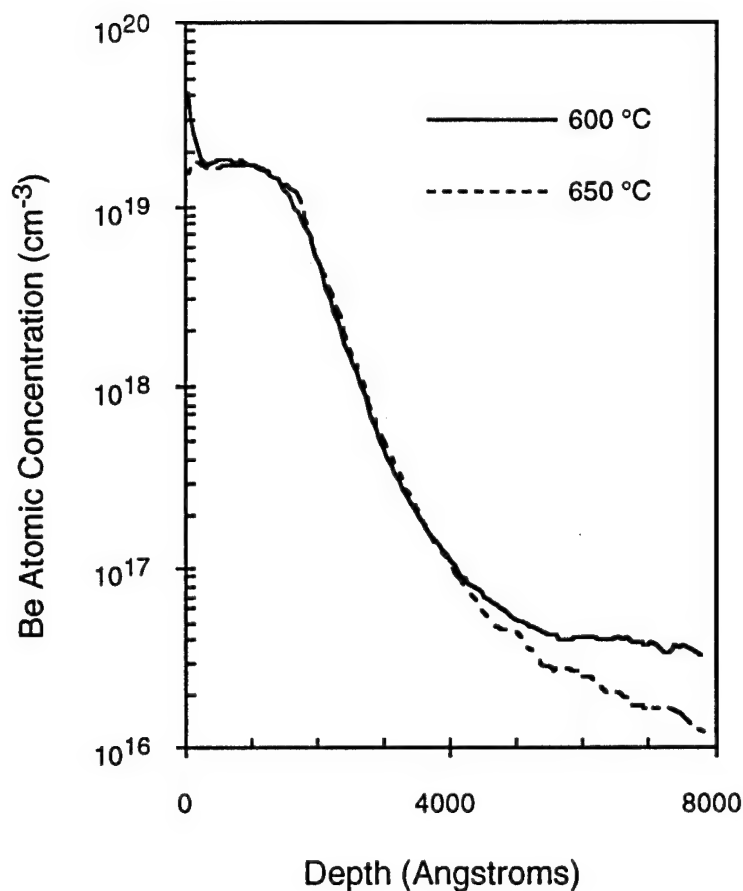


Figure 5.11. Polaron atomic concentration profiles of Be-implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ on InP following RTA at 600 °C or 650 °C for 10 seconds. The implant conditions were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and $E = 50 \text{ keV}$.

Summary statistics were collected on a number of $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ samples using the Polaron. The statistics establish generalized trends for Polaron measurements made on different samples and subjected to variations in implant dose and RTA temperature. These results were obtained from 40 different Polaron measurements - 10 at each of the four dose/temperature combinations.

Figure 5.13 demonstrates the average surface acceptor concentration obtained from the Be implants. These results demonstrated that the average surface concentration is $\bar{N}_A \equiv$

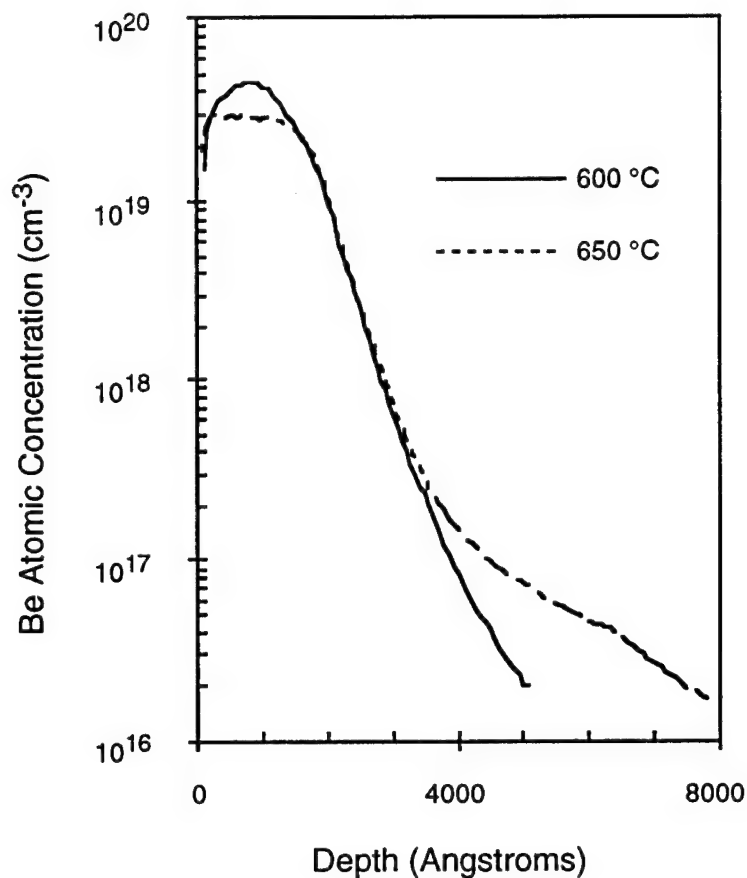


Figure 5.12. Polaron atomic concentration profiles of Be-implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ on InP following RTA at 600 °C or 650 °C for 10 seconds. The implant conditions were $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ and $E = 50 \text{ keV}$.

$2 \times 10^{19} \text{ cm}^{-3}$ irrespective of implant dose or annealing temperature. There is a slightly greater variation in the surface carrier concentration for the lower dosage samples. Also, variation in the surface concentration increases as the anneal temperature is increased for both doses. Therefore, the dose and temperature combinations had little influence on the average surface concentration but did produce an impact in the variation of the surface concentration.

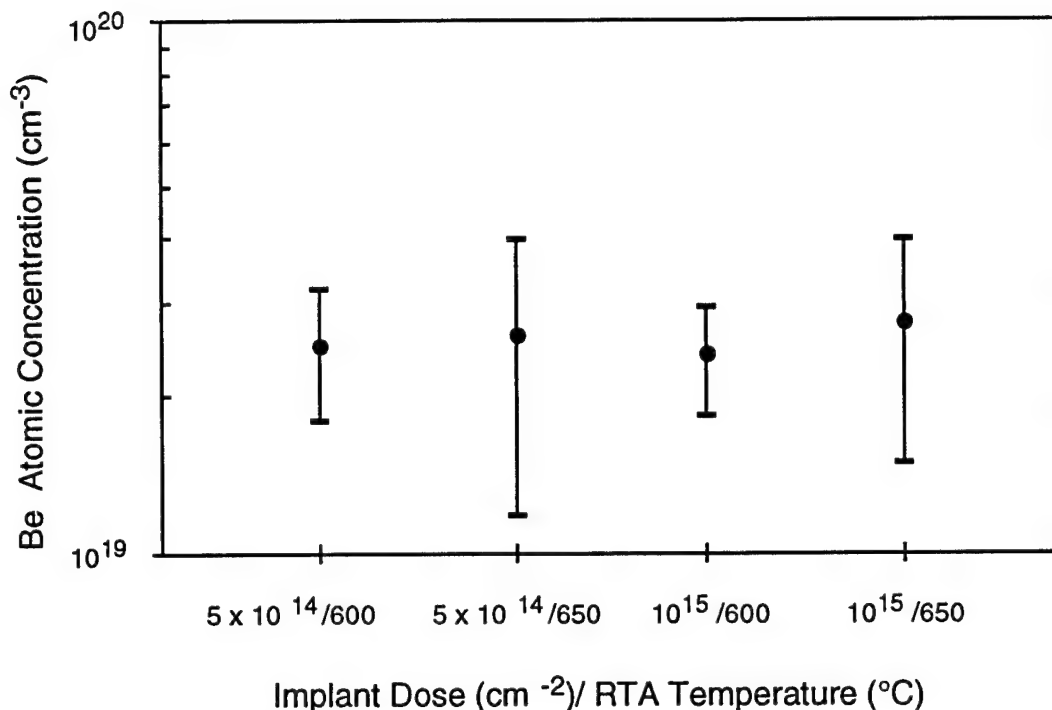


Figure 5.13 Polaron summary statistics of the surface atomic concentration for Be-implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}/\text{InP}$. Profiles from four combinations of implant dose and RTA temperature were obtained. The error bars represent standard deviation. The implant energy was $E = 50 \text{ keV}$ and a 10 second RTA time was used.

Mode depth summary statistics for samples implanted with a dose $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ are demonstrated in Figure 5.14. These samples were subjected to RTA temperatures of 600°C or 650°C . The average mode concentrations were $N_A = 2.0 \times 10^{19} \text{ cm}^{-3}$ and $2.4 \times 10^{19} \text{ cm}^{-3}$ for samples annealed at 600°C and 650°C , respectively. The average mode depths were $d = 804 \text{ \AA}$ and $d = 750 \text{ \AA}$ for samples annealed at 600°C and 650°C , respectively. Thus the average maximum acceptor concentration increased slightly with an increase in RTA temperature while the mode depth decreased slightly. The standard deviations in atomic concentration and mode depth are approximately the same at both temperatures.

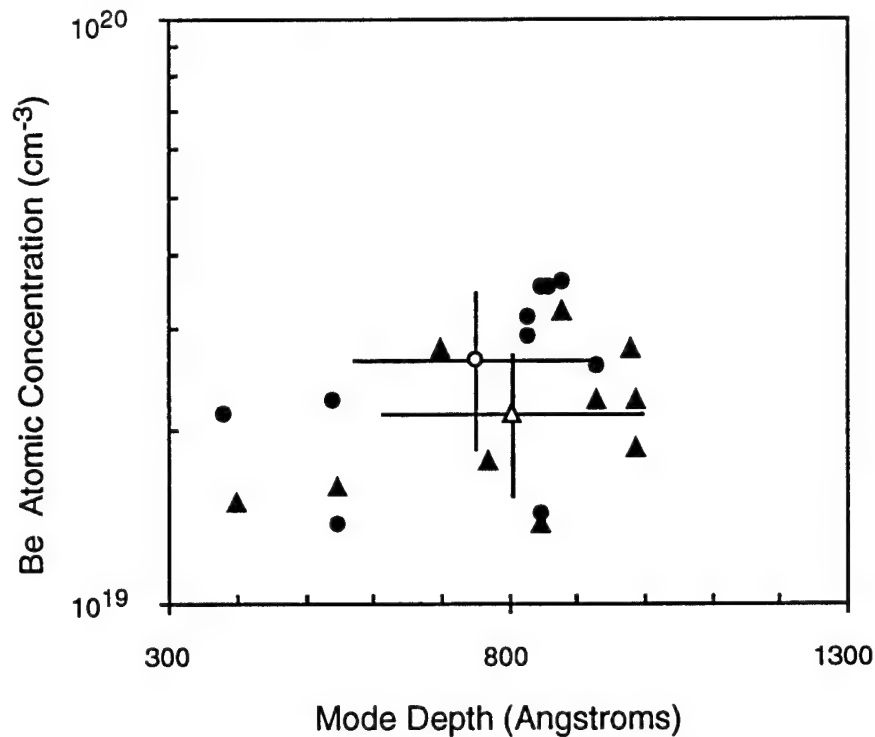


Figure 5.14. Polaron summary statistics of mode depth for Be-implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}/\text{InP}$. Solid triangles and circles represent measurements from samples subjected to a 10 second RTA cycle at 600 °C or 650 °C, respectively. Average values are represented by open symbols. Solid lines represent standard deviation in concentration or depth. Implant conditions were $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, and $E = 50 \text{ keV}$.

Mode depth summary statistics for samples implanted with a dose $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ are demonstrated in Figure 5.15. These samples were subjected to RTA temperatures of 600 °C or 650 °C. The average mode concentrations were $N_A = 4.0 \times 10^{19} \text{ cm}^{-3}$ and $2.9 \times 10^{19} \text{ cm}^{-3}$ for samples annealed at 600 and 650 °C, respectively. The average mode depths were $x = 836 \text{ \AA}$ and $x = 758 \text{ \AA}$ for samples annealed at 600 and 650 °C, respectively. Thus the average maximum acceptor concentration and mode depth decreased with an increase in RTA temperature. The standard deviation in maximum concentration was reduced as the anneal temperature was raised while the standard deviation in mode depth remained essentially the same.

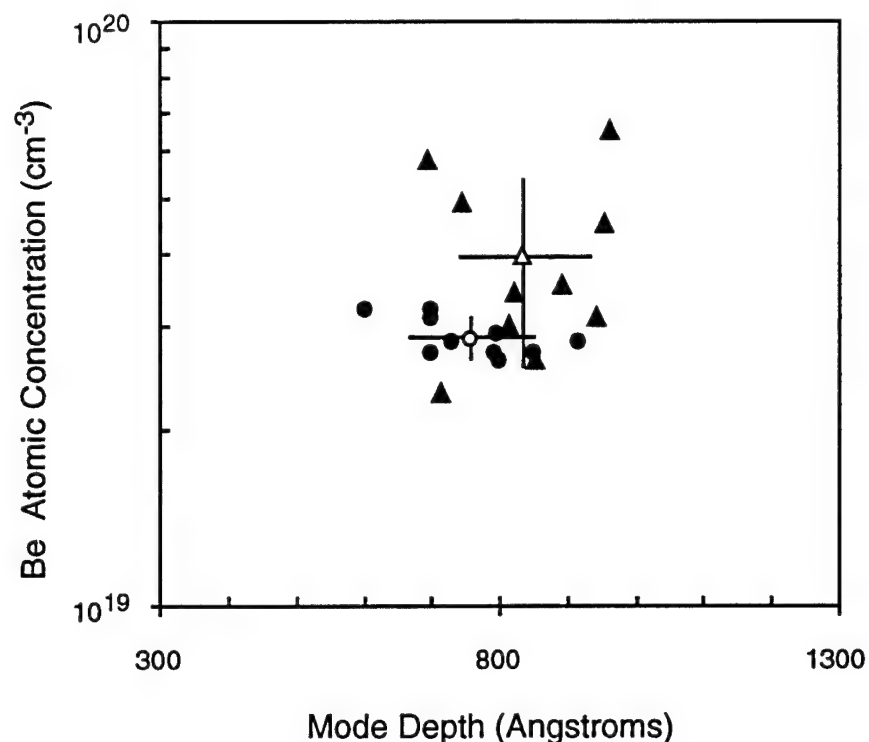


Figure 5.15 Polaron summary statistics of mode depth for Be-implanted GaAs_{0.53}Sb_{0.47}/InP. The solid triangles and circles represent samples subjected to a 10 second RTA cycle at 600 °C or 650 °C, respectively. Average values are represented by open symbols. Solid lines represent standard deviation in concentration or depth. The implant conditions were $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$, $E = 50 \text{ keV}$.

5.4.3 SIMS Characterization Results. SIMS characterization was performed in order to (1) determine the stability of the Ga, As and Sb matrix elements at the Si₃N₄/GaAs_{1-x}Sb_x interface, and (2) to map the Be concentration profiles in the Si₃N₄ and GaAs_{1-x}Sb_x. Degradation of the Si₃N₄ encapsulant layer was reported in Section 5.1 following RTA of Be-implanted GaAs_{0.51}Sb_{0.49} at 700 °C. This degradation appeared as a physical reaction resulting in peeling of the Si₃N₄. An explanation for this degradation reaction is provided by Figures 5.16 and 5.17. These figures are the SIMS profiles of the

Ga, As, and Sb elements in the Si₃N₄ layer following implantation and RTA at 600 °C or 650 °C.* Separate samples from neighboring wafer pieces were used.

Figures 5.16(a) through 5.16(c) are SIMS profiles for GaAs_{0.51}Sb_{0.49} implanted with a Be dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$. A measurable Ga concentration was observed in the Si₃N₄ following implantation. Rapid thermal annealing at 600 °C or 650 °C produced no increase in the Ga signal in the majority of the Si₃N₄ layer. However, the Ga concentration increased on the surface of the Si₃N₄ as the temperature increased. No depletion of the Ga profile beneath the GaAs_{0.51}Sb_{0.49} surface was detected. Therefore, the excess Ga concentration in the Si₃N₄ following implantation and RTA was from the near surface region of the GaAs_{0.51}Sb_{0.49}. The As profiles in Figure 5.16(b) showed a small As trace in the Si₃N₄ after implantation. The As concentration did not increase in the Si₃N₄ as a result of RTA at 600 °C. A slight protrusion of As from the GaAs_{0.51}Sb_{0.49} surface was visible after the 650 °C RTA. No As loss was apparent from the bulk of the GaAs_{0.51}Sb_{0.49} layer. No Sb was detected in the Si₃N₄ in any of the three cases as shown in Figure 5.16(c). The Sb contours remained essentially constant following implantation and annealing.

The SIMS profiles of Figure 5.17(a) through 5.17(c) contain results from Be implantation with a dose of $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$. Gallium was again measured inside the Si₃N₄ following implantation. Rapid thermal annealing increased the Ga content within the Si₃N₄ layer with the maximum amount occurring after RTA at 650 °C. The As concentration also increased in the Si₃N₄ as the RTA temperature was increased from 600 °C to 650 °C. Larger amounts of Ga and As were thus located within the Si₃N₄ layer following implantation at the higher dose. Also, increasing the implant dose caused greater outdiffusion of both Ga and As as the RTA temperature was increased to 600 °C and 650

* SIMS profiling of samples subjected to RTA at 700 °C was not possible due to flaking of the Si₃N₄ as previously described.

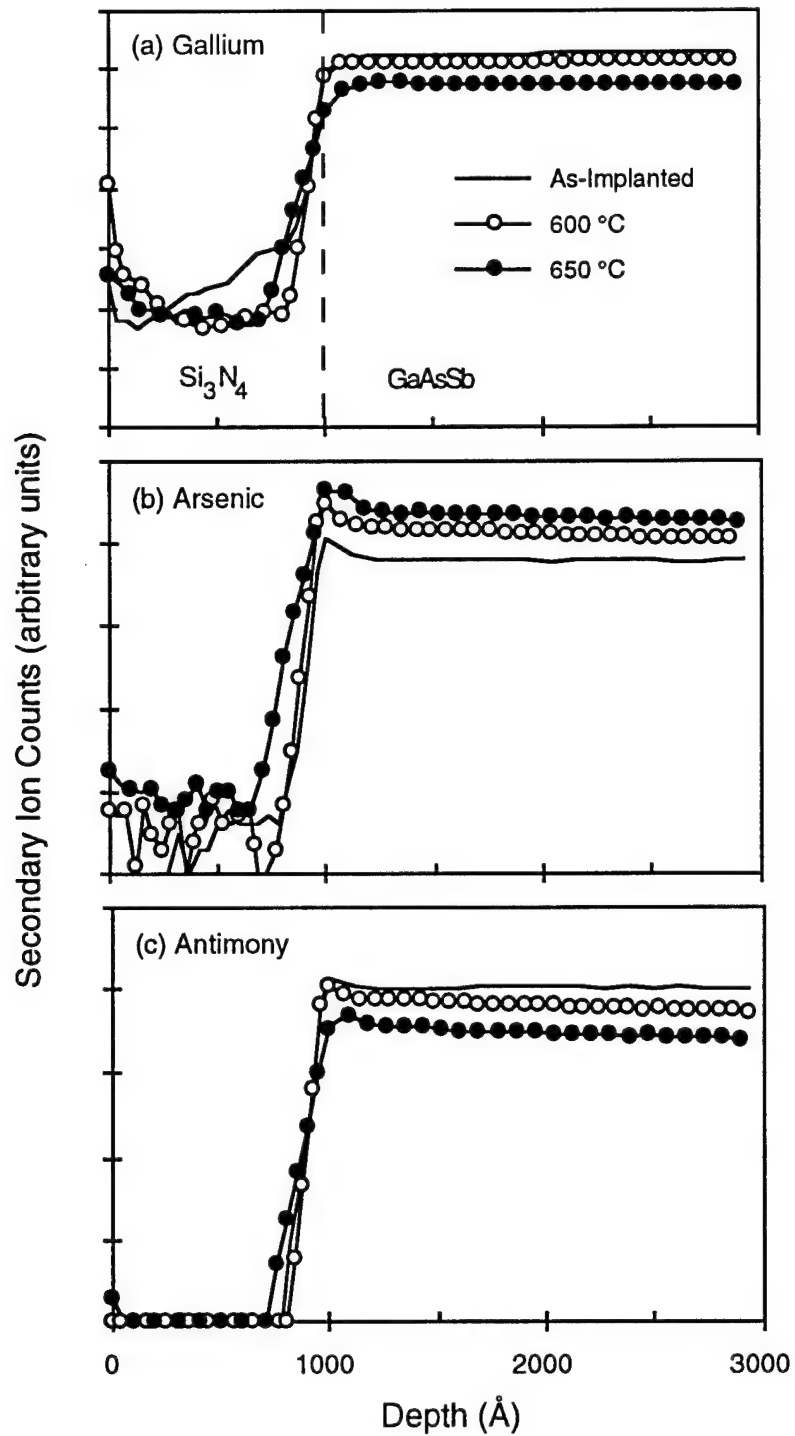


Figure 5.16. SIMS depth profile of a $\text{Si}_3\text{N}_4/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ interface following Be ion implantation and RTA. The Be implant dose was $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, and energy, $E = 50 \text{ keV}$. The Si_3N_4 and $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layers are nominally 1000 Å and 1 μm thick, respectively. The (a) Ga, (b) As and (c) Sb elemental profiles are shown following Be implantation and RTA at 600 °C or 650 °C for 10 seconds.

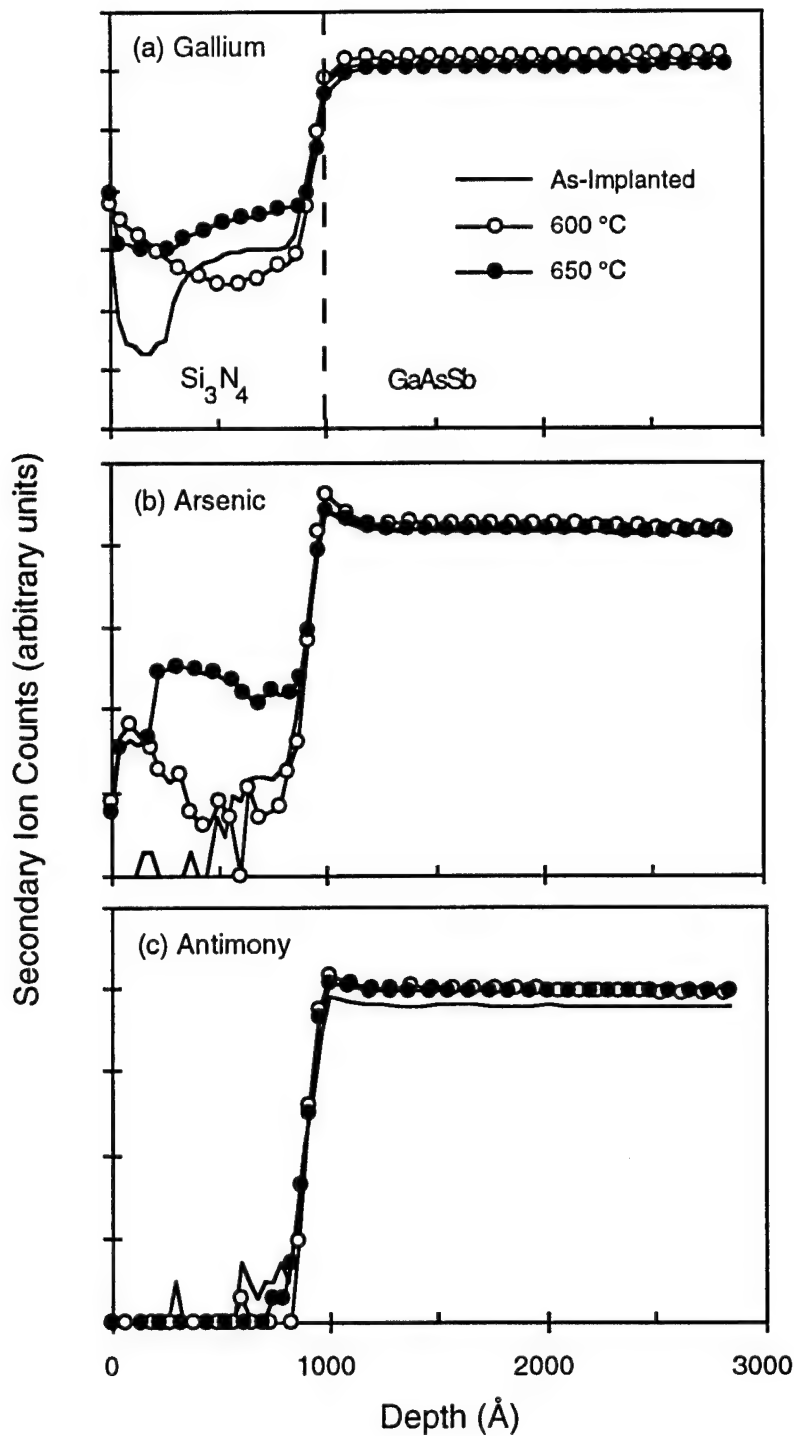


Figure 5.17. SIMS depth profile of a $\text{Si}_3\text{N}_4/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ interface following Be ion implantation and RTA. The Be implant dose was $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$, and energy, $E = 50 \text{ keV}$. The Si_3N_4 and $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layers are nominally 1000 Å and 1 μm thick, respectively. The (a) Ga, (b) As and (c) Sb elemental profiles are shown following Be implantation and RTA at 600 °C or 650 °C for 10 seconds.

°C. Outdiffusion of Sb was not evidenced following implantation nor after RTA. Lack of Sb in the Si₃N₄ is consistent with the SIMS results obtained for the lower implant dose.

SIMS depth profiles in Figure 5.18 demonstrate the Be concentration in the Si₃N₄ and GaAs_{0.51}Sb_{0.49} layers following implantation at $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and subsequent RTA. The Be atomic concentration was calibrated using a uniformly doped GaAs_{0.51}Sb_{0.49}:Be sample as a standard.* The depth scale is referenced from the surface of the Si₃N₄. Enhanced Be yields at the Si₃N₄/GaAs_{0.51}Sb_{0.49} interface may be caused by oxidation of the semiconductor surface and cannot be directly attributed to Be massing. The as-implanted spectrum exhibited a Pearson-type profile. Annealing caused a shift in the peak concentration towards the GaAs_{0.51}Sb_{0.49} surface. Also, the Be concentration increased in the Si₃N₄ following RTA. Tailing of the Be deeper into the GaAs_{0.51}Sb_{0.49} layer occurred following RTA. Like the Polaron profiles, the Be density is above $1 \times 10^{19} \text{ cm}^{-3}$ over the first 1500 Å of the GaAs_{0.51}Sb_{0.49} layer. The roll off characteristics were approximately the same for the two annealing temperatures. The annealed traces have a less steep roll off compared with the Polaron profiles, making resolution of the onset of tailing difficult. This difference may result from nonuniformity in the sputter crater or knock-in of the Be atoms during sputtering with the O₂ beam.

The Be depth profiles obtained by SIMS for $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ are illustrated in Figure 5.19. The Be density near the surface in the GaAs_{0.51}Sb_{0.49} layer was enhanced compared to the lower implant dose sample. The Be density was above $3 \times 10^{19} \text{ cm}^{-3}$ over the first 1500 Å of the GaAs_{0.51}Sb_{0.49} layer. The as-deposited profile exhibited a peak concentration of $5.5 \times 10^{19} \text{ cm}^{-3}$ at a mode depth of 1000 Å into the GaAs_{0.51}Sb_{0.49} layer. The effect of RTA at 600 or 650 °C was similar to that of the $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ dose: (i) the peak concentration shifts towards the GaAs_{0.51}Sb_{0.49} surface, and (ii) tailing is

* The Be concentration in the GaAsSb:Be calibration sample was initially measured by Hall effect.

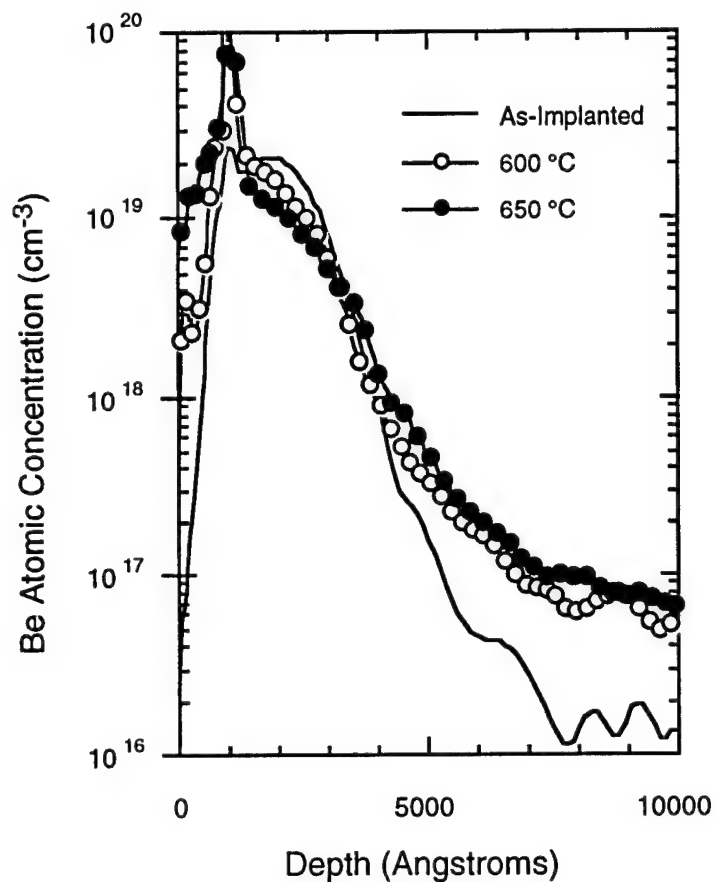


Figure 5.18. SIMS depth profile of Be-implanted $\text{Si}_3\text{N}_4/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layers following RTA. The Be implant dose was $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, and energy, $E = 50 \text{ keV}$. The Si_3N_4 and $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layers are nominally 1000 \AA and $1 \text{ }\mu\text{m}$ thick, respectively. A depth of $d = 0$ represents the Si_3N_4 surface. The elemental profiles are shown as-implanted and following RTA at $600 \text{ }^\circ\text{C}$ or $650 \text{ }^\circ\text{C}$ for 10 seconds.

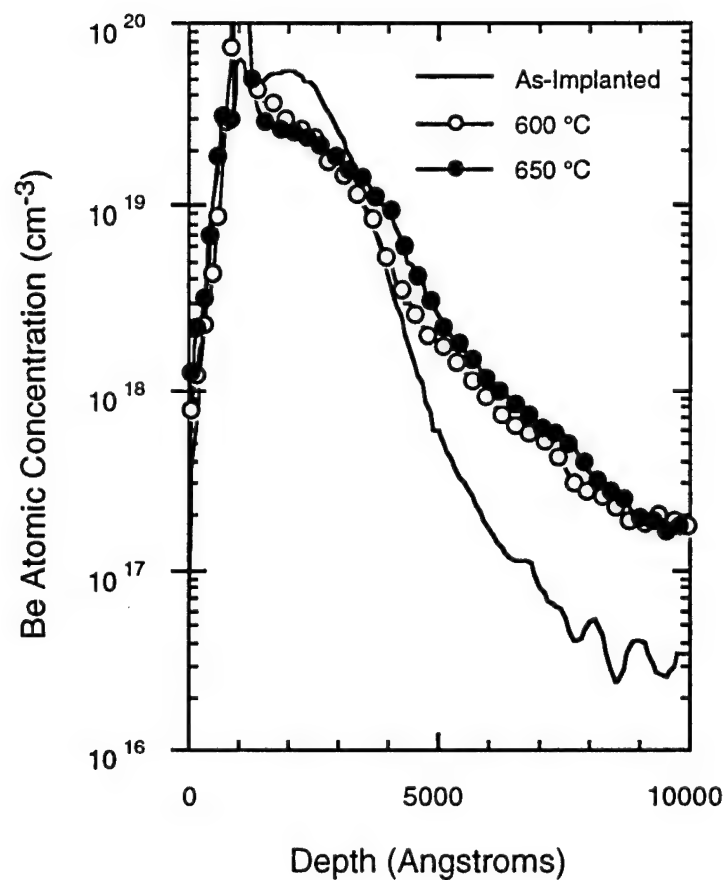


Figure 5.19. SIMS profile of Be-implanted $\text{Si}_3\text{N}_4/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layers following RTA. The Be implant dose was $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$, and energy, $E = 50 \text{ keV}$. The Si_3N_4 and $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layers are nominally 1000 \AA and $1 \text{ }\mu\text{m}$ thick, respectively. A depth of $d = 0$ represents the Si_3N_4 surface. The elemental profiles are shown as-implanted and following RTA at $600 \text{ }^\circ\text{C}$ or $650 \text{ }^\circ\text{C}$ for 10 seconds.

enhanced at depths greater than 3000 Å within the GaAs_{0.51}Sb_{0.49} layer. No evidence of a Be outdiffusion into the Si₃N₄ was observed following annealing.

5.4.4 Photoluminescence Characterization Results. Photoluminescence measurements were taken on Be-implanted GaAs_{0.52}Sb_{0.48}/InP samples. Photoluminescence spectra were obtained at T = 3 K by excitation of the sample with the 0.488 and 0.5145 μm lines of a multi-mode Ar laser. Emission was monitored with a 1.5 m spectrometer and a liquid N₂ cooled Ge photodetector. The implant doses were $Q_0 = 5 \times 10^{14}$ and $1 \times 10^{15} \text{ cm}^{-2}$ at 50 keV through a 1000 Å thick Si₃N₄ layer. The PL was measured after 10 second RTA at temperatures of 600 or 650 °C. The Si₃N₄ was removed using RIE prior to PL spectroscopy.

The PL results are shown in Figures 5.20(a) and 5.20(b). Two distinct peaks were observed in each of the samples. A large peak occurs between 0.79 and 0.80 eV as shown in Figure 5.20(a). A lower intensity shoulder between 0.76 and 0.77 eV is also shown in Figure 5.20(b). The PL excitation intensity was increased from 70 mW/cm² to 1.4 W/cm² in order to adequately observe the lower energy shoulder. Therefore, separate scales are necessary due to the low PL emission of the lower energy shoulder when compared directly with the large peak. These two maxima correspond to (D,A) transitions and are again referred to as the "large" and "small" peaks as in Section 4.3.

A few observations are apparent from Figures 5.20(a) and 5.20(b). First, the linewidths, ΔE, are narrower for the samples implanted with a dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$. These samples produced full-width-half-maximum linewidths of 7.2 and 8.5 meV for T = 600 °C and 650 °C, respectively. The higher dosage samples yielded full-width-half-maximum linewidths of 9.1 and 10.0 meV for T = 600 °C and 650 °C, respectively. Second, the PL emission intensities are reduced for the higher dose samples relative to the lower dose samples. Third, a number of consistencies exist between the large and small peaks. The small peak lies 30 to 33 meV lower than the large peak in three of the four

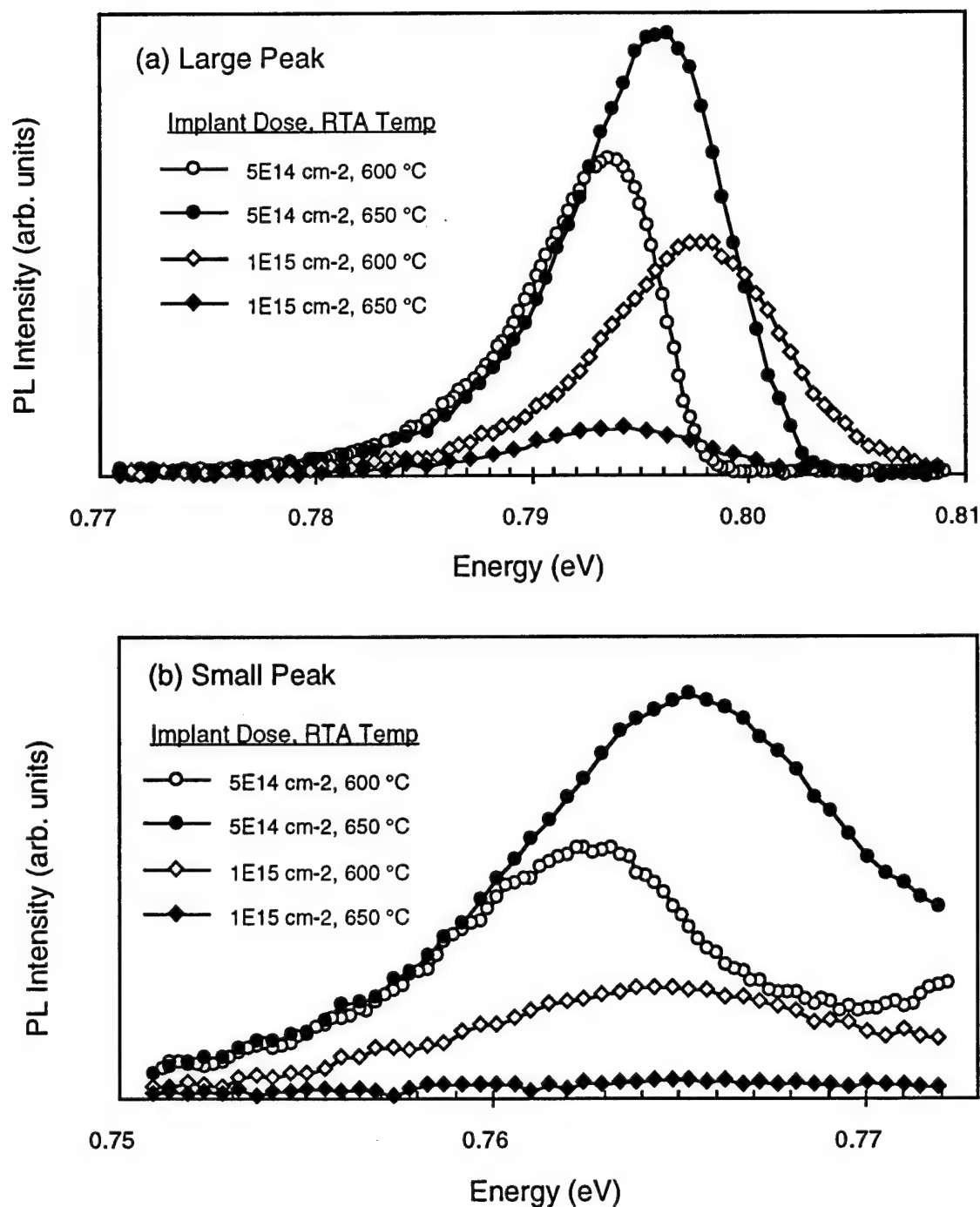


Figure 5.20. Photoluminescence spectra at $T = 3\text{K}$ for Be-implanted $\text{GaAs}_{0.52}\text{Sb}_{0.48}/\text{InP}$. The samples were implanted at $E = 50\text{ keV}$. The RTA time was 10 seconds. The implant dose and RTA temperature are provided in the inset of each graph. Two distinct peaks were observed in each implanted sample: (a) a large peak between 0.79 and 0.80 eV, and (b) a lower intensity peak between 0.76 and 0.77 eV. The spectrometer slit width was $400\text{ }\mu\text{m}$ in all cases with an excitation intensity of (a) 70 mW/cm^2 and (b) 1.4 W/cm^2 .

spectra (the small peak position for the sample with $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$, annealed at $T = 650^\circ\text{C}$ was not measurable). Also, the relative intensities are consistent for both the small and large peaks with respect to implant dose and anneal temperature.

5.5 Discussion of Be Implantation Results

The fact that a high acceptor concentration of $N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$ was obtained over a 1000 \AA depth below the $\text{GaAs}_{1-x}\text{Sb}_x$ surface is the most encouraging aspect of this Be ion implantation study. This doping profile should suffice for a low resistance, alloyed or nonalloyed ohmic contact. RTA activation of the implant occurs at $T = 600^\circ\text{C}$ for both doses. At this temperature, the integrity of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ heterojunction was maintained as shown in Chapter IV. Therefore, implant annealing at $T = 600^\circ\text{C}$ should not damage the heterojunction in the channel region.

There are structural phenomena associated with obtaining the highly doped surface layers. The experimental results demonstrate a transition in the stability of the surface with an increase in dosage from $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ to $1 \times 10^{15} \text{ cm}^{-2}$, and an increase RTA temperature from 600°C to 650°C . Also, the Be acceptor density is both implant dose and RTA temperature dependent. Additionally, tailing of the implant profiles was indicated by both Polaron and SIMS. To simplify analysis of these and other phenomena, the implantation results are analyzed by dividing the implanted structure into three separate regions: (i) Si_3N_4 layer and $\text{Si}_3\text{N}_4/\text{GaAs}_{1-x}\text{Sb}_x$ interface, (ii) near surface in the $\text{GaAs}_{1-x}\text{Sb}_x$ layer ($0 \leq d \leq 3000 \text{ \AA}$), and (iii) deep in the $\text{GaAs}_{1-x}\text{Sb}_x$ layer ($d \geq 3000 \text{ \AA}$).

(i) Si_3N_4 Layer and $\text{Si}_3\text{N}_4/\text{GaAs}_{1-x}\text{Sb}_x$ Interface. The optical micrographs of $\text{GaAs}_{0.5}\text{Sb}_{0.5}$, GaAs and Si dictate that the Si_3N_4 degradation at 700°C is not a function of $\text{GaAs}_{0.5}\text{Sb}_{0.5}$ surface preparation nor Si_3N_4 deposition conditions. No degradation was observed on GaAs surfaces covered with Si_3N_4 . Therefore, the reaction most likely involves the inclusion of Sb in the lattice. The flaking of the Si_3N_4 appears caused by a

reaction which physically cracks and lifts the Si_3N_4 layer but does not chemically react with it. A chemical phase combining the Ga, As or Sb matrix elements and the Si_3N_4 would likely prevent complete removal of the Si_3N_4 by RIE.

The potential for surface destabilization in $\text{GaAs}_{1-x}\text{Sb}_x$ due to elevated temperatures was verified by a previous anneal study [16]. This study did not report a degenerate interaction between Si_3N_4 and non-implanted $\text{GaAs}_{0.45}\text{Sb}_{0.55}$ following annealing at 580 °C for one hour. However, X-ray diffraction results demonstrated a GaAs-rich phase, indicating loss of Sb and phase separation at the surface. The GaAs-rich phase was not observed following removal of the Si_3N_4 , implying phase separation occurred at the surface only. Thus elevating near lattice matched $\text{GaAs}_{1-x}\text{Sb}_x$ to temperatures near $T = 600$ °C causes decomposition at the surface even in unimplanted material. Raising the RTA temperatures above 600 °C increases the risk of decomposition.

The pseudo-binary phase diagram of GaSb-GaAs provides a possible explanation for the observed surface reaction of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ at 700 °C [17]. The phase diagram shows the solidus temperature for $\text{GaAs}_{1-x}\text{Sb}_x$ lies between $710 \leq T \leq 730$ °C for Sb compositions of $0.2 \leq x \leq 1.0$. The solidus temperature decreases as the Sb composition is raised. Above the solidus temperature a mixture of both solid and liquid $\text{GaAs}_{1-x}\text{Sb}_x$ phases exists to approximately 1100 °C for $x = 0.49$. Exposing the samples to a 700 °C thermal cycle likely results in at least partial melting of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. Partial melting of the $\text{GaAs}_{1-x}\text{Sb}_x$ is possible if As outdiffuses from the surface during RTA, and the Sb composition in a particular region is raised above $x = 0.49$. Therefore, the previously reported anneal study [16] and the phase diagram [17] show an onset of surface instability at 600 °C due to phase separation, and an upper thermal limit of 700 °C due to partial melting for non-implanted, near lattice matched $\text{GaAs}_{1-x}\text{Sb}_x$. Ion implantation appears to further destabilize the surface based upon results presented in this dissertation.

The SIMS results of Figures 5.16 and 5.17 pinpoint the sources of surface instability in Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. These SIMS profiles show the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ instability is a function of implant dose and anneal temperature. Some observations are apparent from the two figures. These observations are explained in the subsequent three paragraphs in terms of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ matrix elements

Gallium. An excess of Ga in the Si_3N_4 layer is initiated during implantation and enhanced following RTA. A comparison of the Ga traces of Figures 5.16(a) and 5.17(a) indicates a greater amount of Ga in the Si_3N_4 following implantation at the higher implantation dose. The highest temperature encountered prior to ion implantation is 350 °C - occurring during chemical vapor deposition of the Si_3N_4 . Dissociation of surface Ga from the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ is unlikely to occur at this low temperature. Therefore, the post-implant Ga concentration in the Si_3N_4 is attributed to sputtered Ga atoms, dislodged from the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface during implantation. Sputtering of Ga is also verified by the fact that the higher implant dose caused a greater concentration of Ga to emerge from the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface into the Si_3N_4 following implantation.

Arsenic. A slightly different process appears to occur for As, and indicates diffusion is the main process for As transport into the Si_3N_4 layer. Both doses produced a small As concentration in the Si_3N_4 layer following implantation. Hence, sputtering of As occurred during implantation but was not as prevalent as that of Ga. The As concentration remained essentially constant with respect to RTA temperature for the lower implant dose. However, the larger implant dose produced a greater amount of As in the Si_3N_4 as the RTA temperature was increased to 650 °C. Greater arsenic outdiffusion at an equal RTA temperature indicates increased damage of the Si_3N_4 at the higher implant dose since: (1) the as-implanted As concentration was low in the Si_3N_4 for both doses, (2) a greater amount of grain boundaries potentially exist in the Si_3N_4 after implantation at the higher dose, and (3) outdiffusion was limited to the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface for both doses.

Antimony. No evidence of Sb sputtering or outdiffusion was detected for either dose. Little presence of Sb in the Si_3N_4 indicates the heavier Sb atoms do not sputter during implantation, and may cluster at the $\text{Si}_3\text{N}_4/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface as opposed to outdiffusing during RTA. Antimony is mobile on $\text{GaAs}_{1-x}\text{Sb}_x$ surfaces during MOCVD [16] and MBE [18] growth. Antimony also tends to cluster due to its high sublimation energy and low atomization energy relative to arsenic [18]. Samples grown near 600 °C at reduced growth rates show reduced lattice incorporation of Sb due to the high surface mobility and clustering [16]. Somewhat similar conditions exist during RTA - whereby surface Sb and As atoms are not replenished and As outdiffusion is similar to sublimation. Therefore, clustering of Sb at the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface during RTA appears quite plausible. Outdiffusion did not occur from deep within the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ for any semiconductor element at either implant dosage.

The above results permit conclusions concerning the Si_3N_4 degradation. First, the optical micrographs and SIMS results indicated that damage to the Si_3N_4 layer was initiated during implantation. This damage increased with increasing implant dosage and affects the ability of the Si_3N_4 to behave as an encapsulant during RTA. Second, sputtering of the Ga and As elements from the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface is most likely occurring - particularly Ga. Gallium is the most abundant and lightest element in the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ matrix, making surface sputtering plausible. The sputtering appears to decrease as the atomic mass increases. Post-implant concentrations in the Si_3N_4 and the atomic masses increase in the order: Ga, As, Sb. Third, increased dosage caused greater outdiffusion for both Ga and As as the RTA temperature was increased to 650 °C. Outdiffusion would increase as the temperature is raised above 650 °C to 700 °C. Finally, lifting of the Si_3N_4 at 700 °C is most likely caused by bubbling of sputtered and diffused Ga from within the Si_3N_4 . Gallium has a very low melting temperature ($T_m = 30$ °C) [19]. Localized Ga concentrations would be liquid at room temperature and expand during RTA as the temperature was increased.

The above studies demonstrated that a dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and a 10 second, 600 °C RTA produces the least amount of damage to the Si_3N_4 and the greatest amount of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface stability. An RTA temperature of 600 °C is relatively low for implant activation compared to the anneal temperatures used for GaAs. Rapid thermal annealing of Be-implanted, Si_3N_4 -encapsulated GaAs at temperatures of 900 °C has been demonstrated with no reports of surface degradation [6-9]. Therefore, a much lower temperature ceiling exists for $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ relative to GaAs. The upper thermal limit of 600 °C at 10 seconds also concurs with the requirement for structural integrity of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ SAG HIGFET which exhibited layer degradation at 700 °C due to elemental cross diffusion [20].

(ii) Near Surface Region in the $\text{GaAs}_{1-x}\text{Sb}_x$ Layer ($0 \leq d \leq 3000 \text{ \AA}$). The Polaron, SIMS and PL results permit some conclusions regarding the effects of implantation and annealing on the Be concentration near the $\text{GaAs}_{1-x}\text{Sb}_x$ surface. Clearly, the increase in the implantation dose from $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ to $1 \times 10^{15} \text{ cm}^{-2}$ results in a larger overall concentration of Be within the near surface region. The Polaron results of Figures 5.11 and 5.12 and the SIMS profiles of Figures 5.18 and 5.19 show this result pictorially. Statistically, this fact is borne by the Polaron results of Figures 5.14 and 5.15 where the average concentration at the implant mode increased from $1 - 2 \times 10^{19} \text{ cm}^{-3}$ for the lower dose to $2 - 3 \times 10^{19} \text{ cm}^{-3}$ for the higher dose. Hence, the activated acceptor concentration in this region is high and should contribute to low contact resistance, and a low resistance source/drain regions in $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ SAG HIGFET structures.

Additional conclusions are possible with respect to the implantation and annealing parameters. Before summarizing observations and proposing conclusions, an explanation of mechanisms which affect the Be implantation profile, diffusion and incorporation in $\text{GaAs}_{1-x}\text{Sb}_x$ are presented. Presented are: (1) a basis for the existence of native threading dislocations and (2) the Be incorporation process.

Dislocations in GaAs_{1-x}Sb_x Films on InP Near the Lattice Matched Condition. As shown subsequently, threading dislocations associated with lattice mismatch are likely in GaAs_{1-x}Sb_x epilayers on InP which are within a few atomic percent of the lattice matched composition ($x = 0.49$). Misfit dislocations occur in III-V thin films due to strain relaxation in the lattice when epilayers are grown thicker than the critical thickness [21,22]. During growth, threading dislocations emerge from misfit dislocations at the film/substrate interface and nucleate as strain is relieved [23]. The nucleation produces dislocation lines parallel to the growth direction. A larger degree of lattice mismatch between the substrate and epitaxial film produces a higher misfit dislocation density, and hence a higher density of threading dislocations. Determination of the critical thickness is important in order to determine whether threading dislocations may exist in the implanted GaAs_{1-x}Sb_x films due to lattice mismatch.

The *critical thickness* for an epilayer of GaAs_{1-x}Sb_x sandwiched between two layers possessing the InP lattice constant (i.e. InP or In_{0.52}Al_{0.48}As) is given by [24]

$$h_c = \frac{a_o(x)}{\sqrt{2}\pi f(x)} \cdot \frac{1 - \frac{v(x)}{4}}{1 + v(x)} \cdot \left[\ln\left(\frac{\sqrt{2}h_c}{a_o(x)}\right) + 1 \right] \quad (5.18)$$

where the $a_o(x)$ is the unit cell length, $f(x)$ is the lattice mismatch, and $v(x)$ is the Poisson ratio for GaAs_{1-x}Sb_x - each a function of Sb composition, x . The lattice mismatch is expressed as [22]

$$f(x) = \frac{a_o(\text{InP}) - a_o(x)}{a_o(x)} \quad (5.19)$$

and Poisson's ratio is [24]

$$\nu(x) = \frac{c_{12}(x)}{c_{11}(x) + c_{12}(x)} \quad (5.20)$$

The components $c_{11}(x)$ and $c_{12}(x)$ are the bulk elastic constants and are dependent on the Sb alloy composition, x .

Equation 5.18 was solved recursively to obtain the critical thickness for $\text{GaAs}_{1-x}\text{Sb}_x$ as a function of Sb composition for both sandwiched $\text{InP}/\text{GaAs}_{1-x}\text{Sb}_x/\text{InP}$ epilayers and a single $\text{GaAs}_{1-x}\text{Sb}_x/\text{InP}$ layer. The results of this analysis are shown in Figure 5.21.

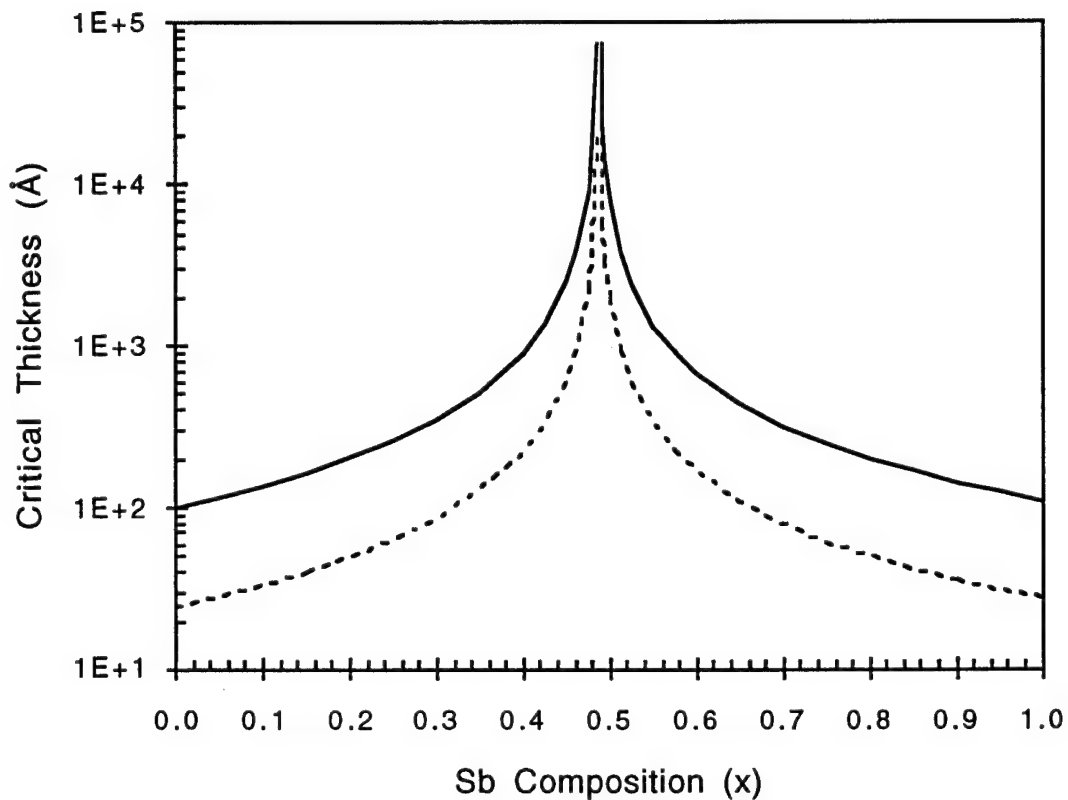


Figure 5.21. Critical thickness as a function of Sb composition for a $\text{GaAs}_{1-x}\text{Sb}_x$ layer on InP. The solid line is for a sandwiched $\text{InP}/\text{GaAs}_{1-x}\text{Sb}_x/\text{InP}$ layer. The dashed line represents a single, $\text{GaAs}_{1-x}\text{Sb}_x$ layer on InP.

All necessary structural and mechanical constants were taken from Reference [25] ($T = 300$ K values). The variables $a_0(x)$, $c_{11}(x)$ and $c_{12}(x)$ were obtained for $\text{GaAs}_{1-x}\text{Sb}_x$ using linear interpolation between GaAs and GaSb values. The critical thickness for the single $\text{GaAs}_{1-x}\text{Sb}_x$ film is simply one-fourth that of the sandwiched layer due to lattice strain accommodation in only one InP layer and geometry factors for misfit dislocations [21].

Figure 5.21 shows that a $1\text{ }\mu\text{m}$, single layer, $\text{GaAs}_{1-x}\text{Sb}_x$ film on InP remains strained over a very narrow range of Sb composition around the lattice matched value ($x = 0.49 \pm 0.01$). The $\text{GaAs}_{1-x}\text{Sb}_x$ films used experimentally were all nominally greater than or equal to $1\text{ }\mu\text{m}$. Therefore, threading dislocations are highly likely following growth in the $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ samples measured by Polaron. Residual threading dislocations would affect diffusion processes following RTA of the $\text{GaAs}_{1-x}\text{Sb}_x$ samples. Threading dislocations may also affect the as-implanted Be implant profiles, diffusion processes and Be incorporation as subsequently explained.

Beryllium Incorporation Process. Beryllium incorporation in $\text{GaAs}_{1-x}\text{Sb}_x$ is explainable in terms of two mechanisms identified in GaAs [9,26,27]. The two processes are the *kick-out* and *dissociative* mechanisms, which are demonstrated pictorially in Figures 5.22 (a) through 5.22(d). These figures show a two-dimensional representation of a localized portion of the $\text{GaAs}_{1-x}\text{Sb}_x$ lattice. Figure 5.22(a) shows a positively charged Be ion residing in an interstitial position within the lattice. Figure 5.22(b) represents a neutral Ga vacancy within the lattice. The Ga vacancy may result from a point defect occurring during growth, in which case a dislodged Ga atom is not present. Dislodging of a Ga atom during implantation may also incur the vacancy. The interstitial Be ion and the Ga vacancy both help describe the two incorporation mechanisms which occur during implantation and annealing.

The *kick-out* mechanism is represented in Figure 5.21(c). A Be ion incorporates on a Ga sublattice site and produces a Ga interstitial atom and two holes. The Ga atom is

removed by kinetic energy during implantation or during RTA when unbonding of the Ga atom from the lattice favors attainment of an equilibrium ratio of interstitial to substitutional Be [9,26]. The kick-out process is described by [27]



The *dissociative* process is similar to kick-out. However, no Ga interstitial is produced from the incorporation of an interstitial Be ion:



Thus interstitial Be ions compete with interstitial Ga atoms for the occupation of the Ga vacancies following implantation. Beryllium incorporation is regulated by the ability of Be or Ga to diffuse to the Ga vacancies, and the density of intrinsic or implant-generated Ga vacancies. Beryllium diffusion is controlled by the implanted concentration and the amount of lattice damage which occurs during implantation. Now that the mechanisms for threading dislocations and Be incorporation were presented, they are applied to conclusions concerning observed experimental results.

The average mode depth and its deviation provide insight on the impact of implant dose. A comparison of Figures 5.14 and 5.15 shows a smaller standard deviation in the mode depth exists for the higher dose case. An average mode depth of $750\text{-}800 \pm 200 \text{ \AA}$ was measured for the lower dose and $760\text{-}840 \pm 100 \text{ \AA}$ for the higher dose. Hence, the average mode depths are essentially the same following annealing while the deviation in the mode depth is halved as the dose was increased. The decreased spreading at the higher dosage may result from increased lattice damage to the $\text{GaAs}_{1-x}\text{Sb}_x$. Light ions such as Be produce narrow, elongated damage tracks [2]. Increasing the dosage increases the density of these damage tracks and reduces crystalline ordering. Implanted ions are less likely to

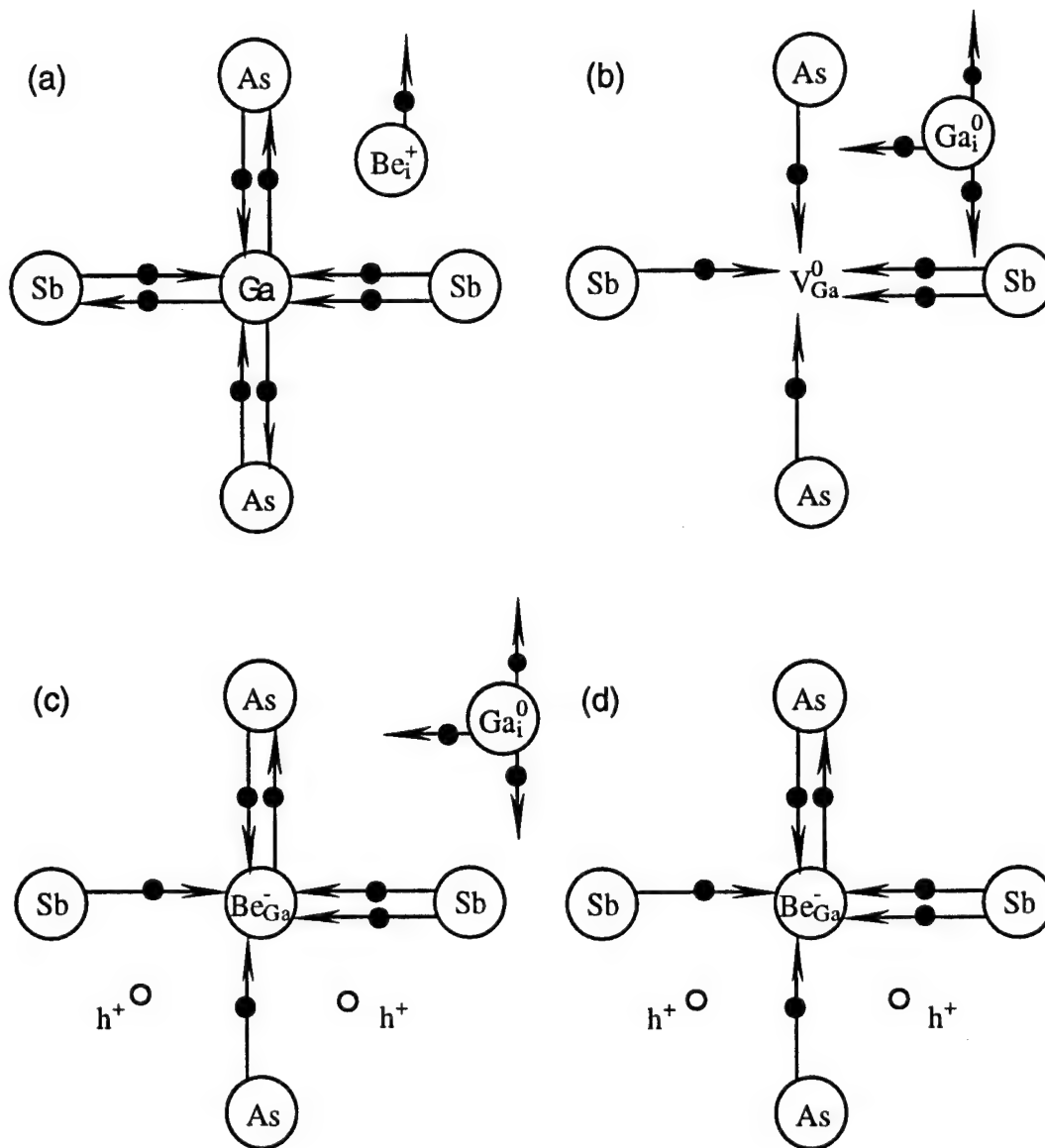


Figure 5.22. Two-dimensional representation of beryllium incorporation in GaAs_{1-x}Sb_x: (a) interstitial Be ion in a GaAs_{1-x}Sb_x host lattice, (b) a neutral Ga vacancy and a neutral, interstitial Ga atom, (c) kick-out mechanism of Be incorporation, and (d) dissociative mechanism of Be incorporation. Electrons are represented by closed circles. Arrows represent bonds originating from a host atom.

travel along crystallographic axes as the dosage is increased. Thus randomness in the resting location of implanted ions is reduced as the dose is increased.

A loss of single crystallinity due to increased dosage may readily explain the decrease in standard deviation of the profile mode following implantation. However, diffusion of Be ions following RTA depends not only on the damage created during implantation but also upon the implanted Be concentration, and native defects which occur during growth due to lattice mismatch. Implantation damage tracks enhance diffusion of interstitial atoms upon annealing. Beryllium diffusion is enhanced as the Be concentration is increased [2,7,9,27]. Enhancement of Be diffusion also occurs if threading dislocations in the as-grown samples remain following implantation and annealing. Therefore, defects (native and implant induced) and the Be concentration itself play a role in the thermal diffusion of the implanted ions. These factors may impact the Be profiles in $\text{GaAs}_{1-x}\text{Sb}_x$ measured by Polaron and SIMS.

Beryllium diffusion indirectly impacts Be incorporation in the lattice due to the competition for Ga lattice vacancies. Beryllium will have an incorporation advantage over Ga under conditions where rapid diffusion occurs and where an absence of interstitial Ga exists. Interstitial Be diffuses rapidly in GaAs with an increase in temperature due to its unbonded state [26]. Additionally, Be diffuses rapidly in regions where damage (i.e. dislocations, grain boundaries, etc.) has occurred without amorphization of the lattice [26]. The diffusivity of Be in GaAs is approximately seven orders of magnitude higher than Ga at 600 °C: $D_{\text{Be}} = 5.5 \times 10^{-13} \text{ cm}^2/\text{s}$ [9] versus $D_{\text{Ga}} = 4.4 \times 10^{-20} \text{ cm}^2/\text{s}$ [25] for Be concentrations of $1 \times 10^{19} \text{ cm}^{-3}$. Therefore, the diffusion of Be is much higher than Ga in an ordered lattice. Beryllium diffusion would additionally increase in a damaged lattice as occurs under high dose conditions. The factors which control Be diffusion, defects and concentration, thus impact Be incorporation as well. These diffusion factors are included in the remaining discussion of the experimental observations.

The average mode depth in the $\text{GaAs}_{1-x}\text{Sb}_x$ samples depended on Be diffusion characteristics related to the implant dose and anneal temperature. In both the Polaron and SIMS results the mode depth shifted towards the $\text{GaAs}_{1-x}\text{Sb}_x$ surface as the anneal temperature was increased, indicating outdiffusion. Similar outdiffusion of implanted Be was previously observed in GaAs [5,9,26] and $\text{Ga}_{0.96}\text{Al}_{0.04}\text{Sb}$ [28] samples. Outdiffusion occurred more readily in high dose ($Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$), low energy ($E \leq 60 \text{ keV}$) Be implants [9]. In general, the diffusivity of Be in GaAs was observed to increase as the dose and temperature were increased [9,26]. Increased diffusivity was linked to increased lattice damage caused by a higher implant dosage [2,9,26].

Surface massing of Be in $\text{GaAs}_{1-x}\text{Sb}_x$ following annealing likely results from a single or combinatorial reaction. First, a lack of Ga atoms at the surface near $d = 0$ favors Be incorporation at the surface. The SIMS results of Figures 5.16(a) and 5.17(a) exhibited a Ga concentration in the Si_3N_4 following implantation. The Ga density in the Si_3N_4 increased with increasing dose and increasing anneal temperature. Therefore, the immediate surface region is Ga deficient after implantation and becomes more deficient as the anneal temperature is increased. Implanted Be ions would not have to compete with interstitial Ga for occupation of Ga vacancies in this region. Thus Be incorporation through the dissociative mechanism is favored. Second, enhanced outdiffusion may occur due to increased damage near the surface ($0 < d \leq 1000 \text{ \AA}$) relative to damage at deeper depths. The implant dosage coupled with the low mass of the Be ion most likely prevent complete amorphization of the surface layer. Previous studies of GaAs and GaSb implantation using Si ($M \approx 28$ atomic mass units) show amorphization of the surface layer requires a threshold dose of $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ [29]. Be ions are lighter ($M \approx 9$ atomic mass units) and would favor isolated disorder regions without complete amorphization if $Q_0 \leq 1 \times 10^{15} \text{ cm}^{-2}$. Therefore, the shift in the Be concentration mode towards the surface may result from enhanced diffusion along grain boundaries and residual threading

dislocations. The enhanced diffusion increases the concentration of Be interstitials near the surface and enhances the probability of Be substitution due to kick-out [26]. Third, oxidation of GaAs surfaces ($0 \leq d \leq 30 \text{ \AA}$) has produced massing of Be at the surface through the formation of BeO_x compounds [7]. Oxidation was observed on as-grown $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surfaces [20] and is also indicated by the enhanced Be signal in the SIMS plots of Figures 5.16 and 5.17. Thus massing of Be at the $\text{GaAs}_{1-x}\text{Sb}_x$ surface due to beryllium oxide formation is conceivable. To summarize: surface massing of implanted Be in near lattice matched $\text{GaAs}_{1-x}\text{Sb}_x$ likely results from: (1) the dissociative mechanism very near the surface ($d \approx 0$) due to an excess of Ga vacancies caused by sputtering of surface Ga during implantation and exacerbated by Ga outdiffusion during RTA, (2) the kick-out mechanism enhanced by interstitial Be diffusion along dislocation tracks in the region $0 < d \leq 1000 \text{ \AA}$, (3) formation of BeO_x compounds due to surface oxidation in the region $0 \leq d \leq 30 \text{ \AA}$.

The PL and Polaron results indicate that Be outdiffusion may assist Be incorporation at the lower dose but increase the interstitial Be concentration at the higher dose. Enhancement of the interstitial Be density and unannealed lattice damage at higher doses are indicated by comparing the PL results of Figure 5.20 and the Polaron results of Figures 5.14 and 5.15. Reduced intensity and wider linewidths were indicated in the PL spectra for the higher dose samples. Additionally, the PL intensity depended on the RTA temperature - increasing for the lower dose and decreasing for the higher dose as the temperature was raised. Thus luminescence from Be (D,A) transitions is enhanced by increasing the RTA temperature at the lower dosage and indicates increased Be incorporation. The reverse is true for the higher dose, luminescence decreases and linewidth increases as the temperature is raised, indicating a larger amount of nonradiative centers due to interstitial Be. Polaron results further support the PL results. The Polaron results show the average, activated Be concentration increased for the lower dose and

decreased for the higher dose as the RTA temperature was increased. Lattice damage and Be interstitial diffusion would both increase with increased dose. Increased RTA temperature would enhance Be diffusion and reduce damage. Hence, reduced luminescence and reduced activation of the Be implant at the higher dose and temperature likely results from incomplete lattice recovery and/or interstitial Be ions acting as defects. These results indicate that the $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ dose annealed at 650 °C produces the most efficient incorporation of Be with the least residual lattice damage.

(iii) GaAs_{1-x}Sb_x Layer with $d \geq 3000 \text{ \AA}$. The Polaron results of Figures 5.8, and 5.10-5.12, and the SIMS results of Figures 5.17 and 5.18 demonstrated a non-Pearson roll off in the Be profile starting at a depth of $d \approx 3000 \text{ \AA}$ from the GaAs_{1-x}Sb_x surface. Two main observations emerge from the decreased steepness of the Be profile: (1) the tailing does not follow any particular trend with respect to dose and temperature, and (2) leveling is worse for GaAs_{0.51}Sb_{0.49}/GaAs compared with GaAs_{0.53}Sb_{0.47}/InP.

A non-Pearson profile tail is indicative of ion channeling [2,26,30]. Channeling occurs when implanted ions are steered along major crystallographic axes with little energy loss. Channeling increases the ion penetration range and reduces the amount of lattice disorder. Lack of channeling is evident through two factors. First, the fact that the tailing profiles are independent of implant dose implies channeling is not predominant. The Polaron, SIMS and PL results indicated a larger amount of lattice disorder near the semiconductor surface in the higher dose samples. Increased disorder due to higher dosage would suppress channeling since the implanted ions are less likely to align with major crystallographic axes after passing through a disordered surface layer [2,26,30]. Therefore, if channeling were present, a higher Be concentration would consistently occur for $d \geq 3000 \text{ \AA}$ in the lower dose samples relative to the higher dose samples. Secondly, implantation occurred at 7° off of the surface normal - a common implant angle for

suppressing ion channeling in GaAs [8,31,32] and GaSb [33] epilayers. Hence, channeling due to the implant angle is not expected.

The decrease in the Be profile slope is most likely due to diffusion through threading dislocations. At 3000 Å, a slight decrease in slope was observed for GaAs_{0.53}Sb_{0.47}/InP as opposed to the concentration plateau obtained in GaAs_{0.51}Sb_{0.49}/GaAs. A comparison between Figures 5.8 and 5.11 demonstrates this fact. The same implant dose, angle, and GaAs_{1-x}Sb_x layer thickness were used in both cases. The equality of these parameters is important when considering implant channeling versus dislocation diffusion. Threading dislocations would dominate in regions where a combination of implant damage followed by solid phase regrowth does not occur. Such a region exists in epitaxial films below the implant damage region and above the substrate. The GaAs_{0.51}Sb_{0.49}/GaAs films have a much higher lattice mismatch than the GaAs_{0.53}Sb_{0.47}/InP combination and are much more prone to a high threading dislocation density. The higher threading dislocation density would enhance Be diffusion towards the substrate. Increased threading dislocation density would explain the lack of variation in the implant tail between the two doses for the GaAs_{0.53}Sb_{0.47}/InP system and the greatly enhanced Be concentration at deeper depths for GaAs_{0.51}Sb_{0.49} on GaAs.

The above arguments are based upon the prevailing data from Polaron, SIMS and PL measurements. Additional XTEM spectroscopy would enhance the above arguments related towards intrinsic dislocations, lattice damage and lattice recovery. Refinement of the Be implant profiles is plausible through adjustment of growth, implant and annealing parameters. These improvements are warranted in situations where the shallowness or abruptness of the implant profile is critical, as in the case of MESFET channels and JFET p-n junctions. These refinements are not as critical for ion implanted source and drain regions. Irregardless, the fundamental goal was achieved - a highly doped surface layer

which is uniform near the surface. Thus p-type ohmic contact formation to Be-doped $\text{GaAs}_{1-x}\text{Sb}_x$ appears promising.

5.6 Chapter V Summary

The results of Be ion implantation in $\text{GaAs}_{1-x}\text{Sb}_x$ were presented in this chapter. The goal was to achieve a highly doped, p-type surface layer. The implantation was characterized by optical microscopy, electrochemical profiling, SIMS and photoluminescence. The method for achieving a uniform, controllable electrochemical etch was demonstrated. Polaron and SIMS results confirm acceptor concentrations of $N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$ within 1000 \AA of the $\text{GaAs}_{1-x}\text{Sb}_x$ surface in samples at or near lattice matched to InP. Optical microscopy and SIMS demonstrated a RTA temperature limit of 650°C for $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and 600°C for $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$. The temperature limitation is imposed by destabilization of the $\text{GaAs}_{1-x}\text{Sb}_x$ surface through Ga sputtering during implantation, and Ga and As outdiffusion during RTA. The highly doped p-type surface layer occurs at a RTA temperature below the threshold temperature for interlayer degradation in $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFETs (Chapter IV). The ion implantation results are promising for ohmic contact formation in ion implanted source/drain regions with $\text{GaAs}_{1-x}\text{Sb}_x$ cap layers as subsequently examined in Chapters VI and VII.

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VI. Au/Zn/Au Alloyed Ohmic Contact to GaAsSb

6.1 Introduction

Motives supporting use of Au/Zn/Au as an ohmic contact to GaAs_{1-x}Sb_x were reviewed in Section 3.2.3.2. These incentives include the potential for achieving low contact resistance as per previous successes on p-type GaAs, and the necessity of evaluating this conventional metallization on GaAs_{1-x}Sb_x for comparison with other III-V ohmic contacts. These and other issues are addressed in the following sections.

Section 6.2 provides specific parameters and procedures used in MBE growth, TLM pattern fabrication and testing. Section 6.3 presents the results of electrical testing on the Au/Zn/Au contact. First presented are TLM and SEM results following isochronal RTA over a sequential temperature range. Also, results from TLM measurements under varying ambient temperature are provided. These measurements permit determination of metal-semiconductor barrier height, and the temperature dependence of sheet resistance and contact resistance. The sheet resistance obtained by TLM is compared with temperature dependent, Hall effect measurements of sheet resistance. The combination of TLM and Hall measurements separates the contributions from the semiconductor and metal-semiconductor regions to the total contact resistance. The Hall mobility is phenomenologically modeled with respect to temperature in order to determine scattering mechanisms which effect the hole mobility in highly doped, Be-implanted GaAs_{1-x}Sb_x.

Section 6.4 provides microstructural characterization results. A number of characterization methods were used to provide complete characterization of Au/Zn/Au-GaAs_{1-x}Sb_x reactions. These methods include atomic force microscopy (AFM), Auger electron spectroscopy (AES), X-ray diffraction (XRD), cross-sectional transmission electron microscopy (XTEM), selected area diffraction (SAD) and energy dispersive X-ray

analysis (EDX). These spectroscopies provide a complete combination for analyzing contact surface morphology and interfacial reactions.

Electrical and microstructural measurements prove Au/Zn/Au is thermally unstable at $T \geq 250$ °C. Hence Au/Zn/Au is unsuitable as an ohmic contact to Be-implanted GaAs_{1-x}Sb_x source/drain regions of the In_{0.52}Al_{0.48}As/GaAs_{1-x}Sb_x HIGFET. The sources of contact degradation are subsequently addressed.

6.2 Ohmic Contact Preparation and Characterization Specifications

The GaAs_{1-x}Sb_x samples were grown by MBE on 2" diameter, semi-insulating InP:Fe substrates. A substrate temperature of 500 °C was used at a rotation of 20 rpm. The GaAs_{1-x}Sb_x active layer thickness was between 3000 Å and 5000 Å depending on the sample grown.* Following growth, TLM patterns were fabricated. TLM mesas were defined using a layer of PMMA photoresist followed by 1400-17 photoresist. TLM mesas were formed by wet chemical etching through the GaAs_{1-x}Sb_x active layer to the InP substrate using H₃PO₄:H₂O₂:H₂O:L-Tartaric acid (1:1:8:0.4) with an approximate etch rate of 150 Å/s. This etch is highly selective - it does not etch the InP substrate. Thus a high degree of thickness uniformity was achieved on the TLM mesas across each sample. Photoresist layers were removed using acetone following mesa etching.

The samples were next patterned for Be ion implantation in the mesa regions. The combined thicknesses of a Si₃N₄ layer and a photoresist layer were used to ensure pad-to-pad electrical isolation and prevent Be implantation in the substrate. Sample surfaces were cleaned using a wet chemical solution of HCl:H₂O (1:20) then NH₄OH:H₂O (1:10) for 30 seconds each. A 60 second, H₂O rinse was used after each dip. A 1000 Å Si₃N₄ layer was then deposited over the mesa and exposed substrate surfaces using PECVD at 350 °C. A single layer of Waycoat 28 (negative) photoresist was next spun over the surface to a

* This layer thickness was selected as thick enough to accommodate the Be implantation profiles shown in Chapter V but not too thick to cause breakage in metal which overlays the TLM mesa from the substrate.

thickness of approximately 1.8 μm . Realignment to the TLM mesas was made, and the negative photoresist was exposed over the mesa. Thus, prior to implantation, only the Si_3N_4 layer was above the mesa region while both Si_3N_4 and Waycoat 28 layers were above the InP substrate. Beryllium ion implantation was then performed at $E = 50 \text{ keV}$, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, and at 7° off-axis. Following implantation, the photoresist layer was stripped. The samples were subjected to RTA at 600°C for 10 seconds. The RTA method and subsequent Si_3N_4 stripping were the same as described in Section 5.3.

Regions requiring Au/Zn/Au metallization were next defined, prior to metal deposition. Two layers of photoresist were deposited and patterned. The first and second photoresist layers were PMMA and 1400-17 with nominal thicknesses of 15,000 \AA and 4,500 \AA , respectively, as measured by a Tencor Dektak profilometer. Gold and Zn layers were thermally evaporated using an Edwards E306A system. Before deposition, layer thicknesses were calibrated by depositing individual layers of Au or Zn and measuring with a Tencor Dektak profilometer. Also, prior to deposition, the sheet resistivity of individual Au and Zn layers were measured by four-point probe. The resistivity ranges over six samples were $2.6 \leq \rho_{\text{Au}} \leq 4.5 \mu\Omega\text{-cm}$, and $13.6 \leq \rho_{\text{Zn}} \leq 17.2 \mu\Omega\text{-cm}$. These resistivity values are near to nominal, reported values of $\rho_{\text{Au}} = 2.4 \mu\Omega\text{-cm}$, and $\rho_{\text{Zn}} = 5.92 \mu\Omega\text{-cm}$ [1]. Deposition pressures were between 1×10^{-6} and 5×10^{-6} torr. Liftoff of the photoresist layers left Au/Zn/Au metallization on the substrate pads and TLM surfaces only.

Rapid thermal annealing and DC testing of the TLM patterns were next accomplished. RTA was performed in a Heatpulse 610 system in a forming gas ambient (5% H_2 , 95 % Ar) with a 10 sccm flow. The samples were placed face down on top of a GaAs wafer. Varying RTA time or temperature was used as subsequently described. Automated TLM measurements were made using an Electroglas 2001X microprobe station. The TLM spacings were $L = 5, 9, 13, 17$ and $21 \mu\text{m}$ as measured by both SEM and a calibrated optical microscope. The length and width of the metallization pads on the mesa

surface were $W = 18 \mu\text{m}$ and $d = 39 \mu\text{m}$, respectively. Linear regression was used to measure the contact resistance (R_c), specific contact resistance (ρ_c), and sheet resistance (R_{sh2}). Linear regression fits with correlations greater than 0.999 were used to calculate average resistance values. The resistance between each TLM pad was measured by forcing a 1 mA current and measuring the corresponding voltage. Forcing currents as low as 10 μA were used with no change in the measured resistance values, ensuring no prevalence of current crowding. Subsequently reported values represent at least 60 TLM sites.

Microstructural characterization was obtained through various profiling and spectroscopic techniques. Characterization specifications are provided in the appropriate section for each method.

6.3 Electrical Characterization and Scanning Electron Microscopy Results

6.3.1. TLM and SEM Results. The initial set of Au/Zn/Au depositions had the following layer thicknesses: 50/200/3000 Å. The 50 Å Au layer is used to promote Zn adhesion to the $\text{GaAs}_{1-x}\text{Sb}_x$. The thinness of the layer should also permit easy diffusion of Zn into the $\text{GaAs}_{1-x}\text{Sb}_x$. The Zn thickness was selected based upon previous results on GaAs [2-7] and GaSb [8-10]. Zinc layer thickness varied between 100 Å and 500 Å in these reports. The 3000 Å top layer of Au was chosen as a thickness suitable for wire bonding.

Two $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ samples with varying Be implant dose, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ or $1 \times 10^{15} \text{ cm}^{-2}$, were initially studied. The Au/Zn/Au RTA temperature range was $250 \leq T \leq 450 \text{ }^\circ\text{C}$ with a constant anneal time of 30 seconds. This temperature range was used to bracket Au/Zn alloy temperatures used for GaAs [References 2, 4, and 7 used $400 \leq T \leq 450 \text{ }^\circ\text{C}$] and GaSb [References 8-10 used $300 \leq T \leq 430 \text{ }^\circ\text{C}$]. Changes in the surface morphology of the contact metallization on the TLM mesa were observed following the isochronal anneal cycles. Surface morphology changes were the same for both implant

doses. Following annealing at 250 °C the Au/Zn/Au surface on the TLM mesa changed from a gold to a grey-gold metallic luster. Annealing at 275 °C caused the contact surface to become increasingly greyish in appearance. After annealing at 300 °C a fairly uniform layer, approximately 2 μm in width, diffused from the contact edge onto the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface in the TLM gaps. Figure 6.1(a) contains a SEM micrograph of two Au/Zn/Au contacts after annealing at 300 °C. The metal contacts are separated by the 13 μm gap on the TLM mesa. The laterally diffusing surface layer is evidenced by the lightly shaded region extending from the edge of the contact onto the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The surface layer continued to spread across the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ as the RTA temperature was increased to 325 °C and 350 °C. Also, the surface morphology at the edge of the Au/Zn/Au contact roughened as the temperature was increased to 350 °C. The surface layer fully traversed the 13 μm TLM gap following RTA at 350 °C. Electrical shorting across the 13 μm gap then occurred. The surface of Au/Zn/Au bonding pads on the InP substrate did not change color or morphology over the annealing temperature range of 250 °C to 350 °C.

The TLM characterization results are demonstrated in Figures 6.2(a) through 6.2(d) for the two $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ samples. The average contact resistance (R_c) is demonstrated in Figure 6.2(a) along with error bars indicating standard deviation. The average specific contact resistance is shown in Figure 6.2(b). A slight reduction in the contact resistance was measured following annealing at 250 °C, and an increase was measured following RTA at 275 °C. After annealing at 300 °C, the average contact resistance decreased. However, some of the measured R_c values were negative following RTA at 300 °C. Almost all of the measured R_c values were negative after the 325 °C anneal. Good correlation to linear regression was not achieved on any of the TLM sites following annealing at 350 °C. Physically, this lack of correlation was caused by electrical shorting between the Au/Zn/Au pads spanning the 5, 9 and 13 μm TLM gaps. The $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ sheet resistance between the TLM pads, shown in Figure 6.2(c), remained essentially

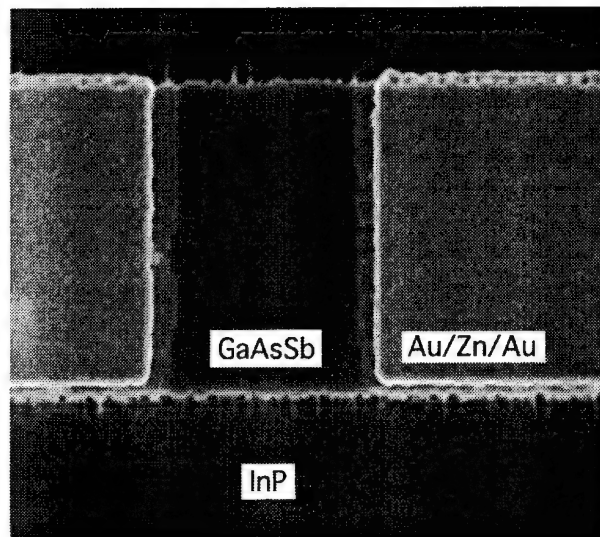


Figure 6.1. Scanning electron micrograph of Au/Zn/Au and GaAs_{0.51}Sb_{0.49} surfaces on the TLM mesa following RTA at 300 °C. Au/Zn/Au metal pads are at each side of the figure while a 13 μm , GaAs_{0.51}Sb_{0.49} gap lies between. The InP substrate surface lies at the top and bottom of the micrograph. The diffusive surface layer appears as the light region on the GaAs_{0.51}Sb_{0.49} between the edges of the Au/Zn/Au metal.

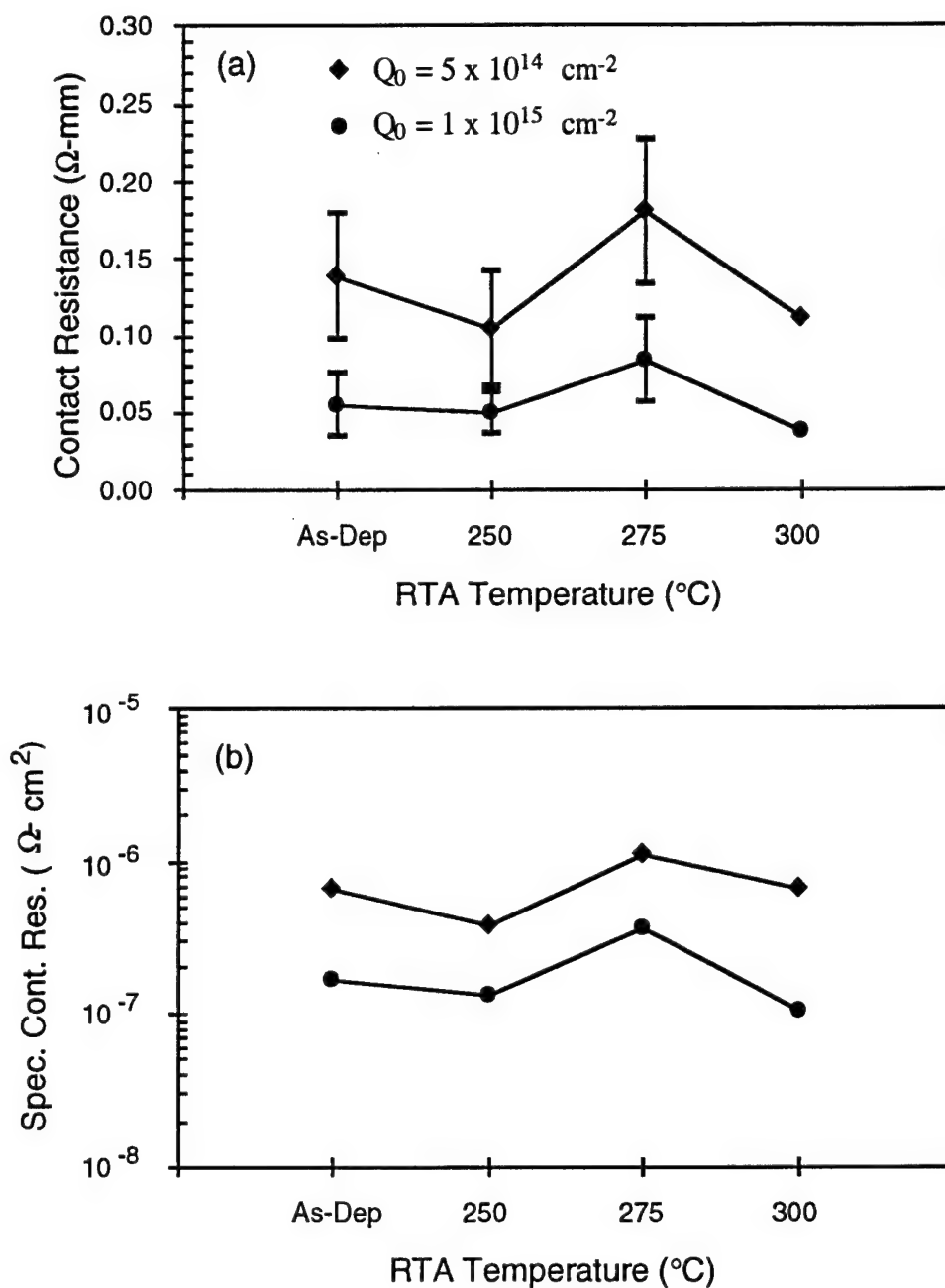


Figure 6.2. Room temperature TLM results for Au/Zn/Au (50/200/3000 Å) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ as a function of RTA temperature: (a) contact resistance (R_c , $\Omega\text{-mm}$), and (b) specific contact resistance (ρ_c , $\Omega\text{-cm}^2$). Two, separate Be implant doses were used, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ or $1 \times 10^{15} \text{ cm}^{-2}$. Isochronal annealing (30 seconds) was sequentially performed on the two samples.

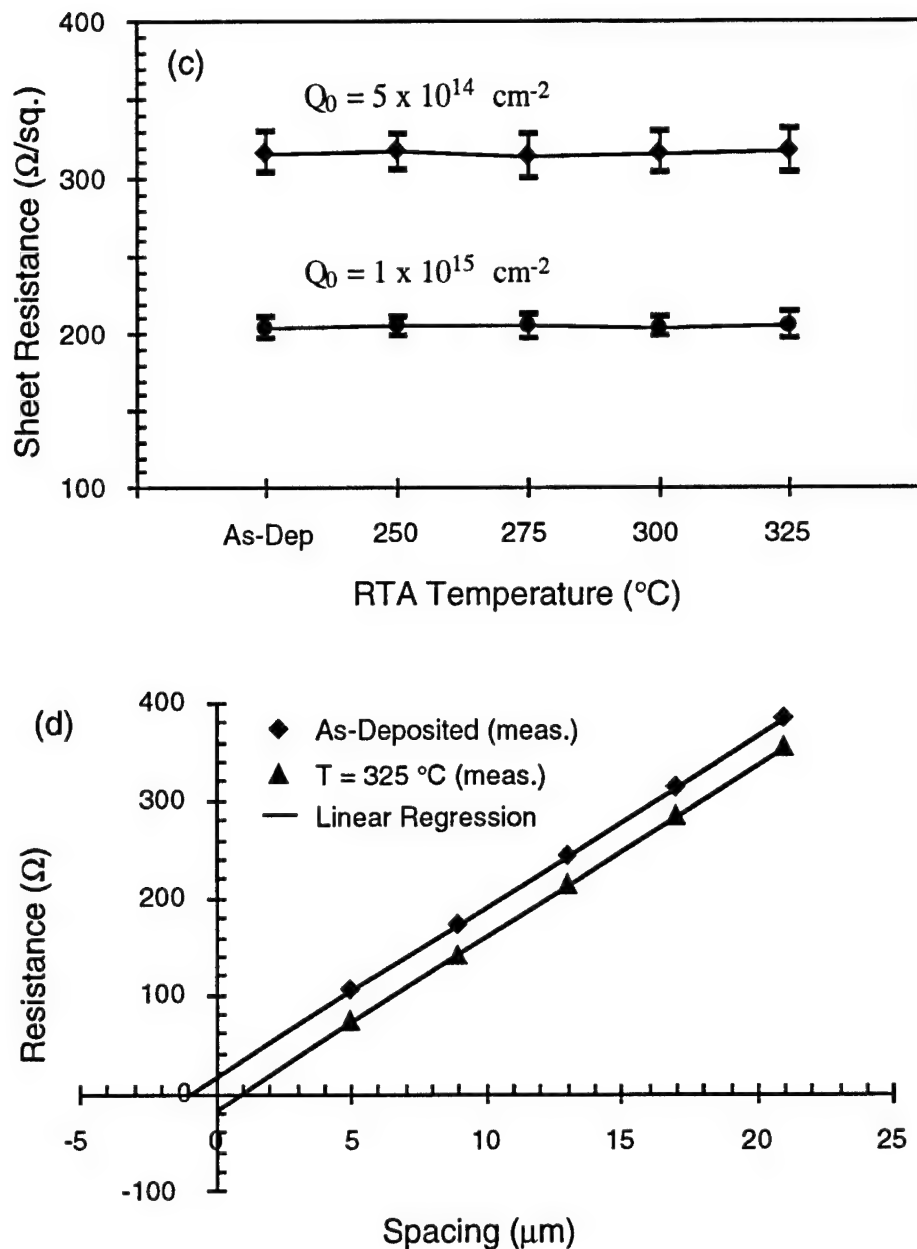


Figure 6.2 (cont.). Room temperature TLM results for Au/Zn/Au (50/200/3000 \AA) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ as a function of RTA temperature: (c) sheet resistance (R_{sh2} , Ω/square). Two, separate Be implant doses were used, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ or $1 \times 10^{15} \text{ cm}^{-2}$. Isochronal annealing (30 seconds) was sequentially performed on the two samples. Measured resistance values are shown in (d) as a function of TLM gap spacing for the lower implant dose sample. The discrete data points were measured following Au/Zn/Au deposition or RTA at 325 $^{\circ}\text{C}$. Linear regression fits to the discrete data points are shown as straight lines.

constant through RTA at 325 °C. Figure 6.2(d) presents measured resistance as a function of TLM pad spacing. The as-deposited data points extrapolate to positive values of contact resistance and transfer length, allowing conventional use of the TLM method. The resistance axis indicates a negative value when extrapolation is performed from the resistance data points representing $T = 325$ °C. This figure graphically shows the decrease in R_c to negatively measured values and the corresponding invariance in sheet resistance as the RTA temperature is increased.

A couple observations are apparent from Figure 6.2. First, an encouraging result was the low, as-deposited, specific contact resistance ($1 \times 10^{-7} < \rho_c < 1 \times 10^{-6} \Omega\text{-cm}^2$) for either implant dose. Thus the lower dose is suitable for a low resistance ohmic contact without alloying. Second, observed changes in surface appearance and contact resistance appear correlated. A decrease in the contact resistance occurred at 250 °C when the color of the Au/Zn/Au surface changed. A sharp decrease in the contact resistance and the laterally diffusing surface layer were both observed after RTA at $T = 300$ °C. Clarifying the causes of both the rapid decrease in R_c to negative values and the source of the laterally diffusing surface layer were deemed necessary.

A number of steps were next taken to resolve or control the sources of negative resistance readings. Negative R_c values may result from (1) using artificially high TLM gap spacings in calculations, (2) errors in measuring the raw resistance values and/or (3) lateral surface diffusion effectively reducing the resistance measured between the TLM gap spacings. Sources (1) and (2) are sources of measurement error. Source (3) is a product of the particular metal/semiconductor system selected.

Sources (1) and (2) are presently addressed. Meticulous efforts were taken to verify the quality of the TLM measurement. First, selected TLM spacings were remeasured before and after annealing using both an SEM and an optical microscope. In all cases, the spacings were the designed values of $L = 5, 9, 13, 17$ and $21 \mu\text{m}$. Thus inaccuracy due to

error in the TLM spacings was not possible, ruling out source (1). Second, the automated resistance measurements were repeated with manual measurements on selected TLM sites. An Alessi probe station was used in conjunction with either a HP 3455A digital multimeter (DMM) or a Tektronix curve tracer. The DMM and curve tracer resistance measurements were within $\pm 4\%$ of the resistance values initially measured by automated probing. Linear regression of experimental data again extrapolated to negative R_c values after the 325 °C anneal. Therefore, TLM measurements using the Electroglas 2001X automated microprobe system were demonstrated as accurate and source (2) was eliminated as a possibility.

Additional Au/Zn/Au samples were processed and tested in an attempt to control the laterally diffusing surface layer [source (3)]. Zinc was considered as the most likely source of the diffusing surface layer. Therefore, efforts to control Zn diffusion were attempted using a reduced RTA time and reduced Zn layer thickness. The following approach was taken:

- (i) Reverify the isochronal annealing results, again using a 200 Å Zn layer and 30 second anneals.
- (ii) Reduce the anneal time to 5 seconds to prevent time-dependent lateral diffusion.
- (iii) Reduce the Zn layer thickness to 100 Å and coprocess the Au/Zn/Au contact on both Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$ and MBE grown GaAs:Be. These approaches were performed in order to reduce the Zn concentration in the contact layer, and apply the Au/Zn/Au to GaAs:Be to determine the intrinsic quality of the deposited metal.

The results are subsequently summarized. Each sample was implanted with a beryllium implant dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$. The processing and implantation methods of Section 6.2 were used in each case.

TLM results following isochronal RTA using a Au/Zn/Au contact on GaAs_{0.52}Sb_{0.48} with a 50/200/3000 Å layer configuration are shown in Figure 6.3(a) and 6.3(b). In Figure 6.3(a) the 30 second anneal time was repeated while in Figure 6.3(b) the anneal time was reduced to 5 seconds. Again a very low, as-deposited average R_c was obtained in both samples ($R_c \leq 0.05 \Omega\text{-mm}$).^{*} The contact resistance continually decreased to negative values as the RTA temperature was raised from $T = 225^\circ\text{C}$. Lateral surface diffusion was observed on both samples starting at $T = 275^\circ\text{C}$. The sheet resistance in both cases remained essentially constant throughout the annealing temperature range. Constancy in the sheet resistance indicates that the resistivity of the GaAs_{0.52}Sb_{0.48} is not changing in the regions between Au/Zn/Au contacts. Consequently, the lateral diffusion occurs across the mesa surface and does not penetrate deeply into the GaAs_{0.52}Sb_{0.48}. These results show that the lateral diffusion was repeatable using a 200 Å Zn layer, and is not eliminated by alloy times as low as 5 seconds.

The Au/Zn/Au was next coprocessed on both MBE grown GaAs:Be and Be-implanted GaAs_{0.51}Sb_{0.49} using a reduced Zn layer thickness of 100 Å. The TLM characterization results are shown in Figure 6.4 for GaAs:Be. The GaAs:Be sample contained a 1000 Å, uniformly doped layer of GaAs:Be ($N_A = 1 \times 10^{19} \text{ cm}^{-3}$) grown on semi-insulating GaAs. The figure shows that the contact resistance is well behaved with respect to anneal temperature. Minimum contact resistances of $R_c = 0.39 \Omega\text{-mm}$ ($\rho_c = 1.55 \times 10^{-6} \Omega\text{-cm}^2$) were obtained following annealing at $T = 350^\circ\text{C}$. This specific contact resistance value is comparable to a previously reported value for Au/Zn/Au on GaAs:C where $\rho_c = 3.6 \times 10^{-6} \Omega\text{-cm}^2$ for $N_A = 4 \times 10^{19} \text{ cm}^{-3}$ [7]. A wide anneal temperature range, $225 \leq T \leq 500^\circ\text{C}$, was demonstrated on the GaAs:Be sample. None of the R vs L

^{*} The specific contact resistance ($\rho_c, \Omega\text{-cm}^2$) is not shown since it is calculated from measurement of the transfer length ($L_T, \mu\text{m}$). Since L_T is one-half of the length axis intercept, a negative measured value of R_c nullifies the meaning of ρ_c taken by the TLM method. Henceforth, the specific contact resistance will not be shown in instances where a negative value of R_c is measured.

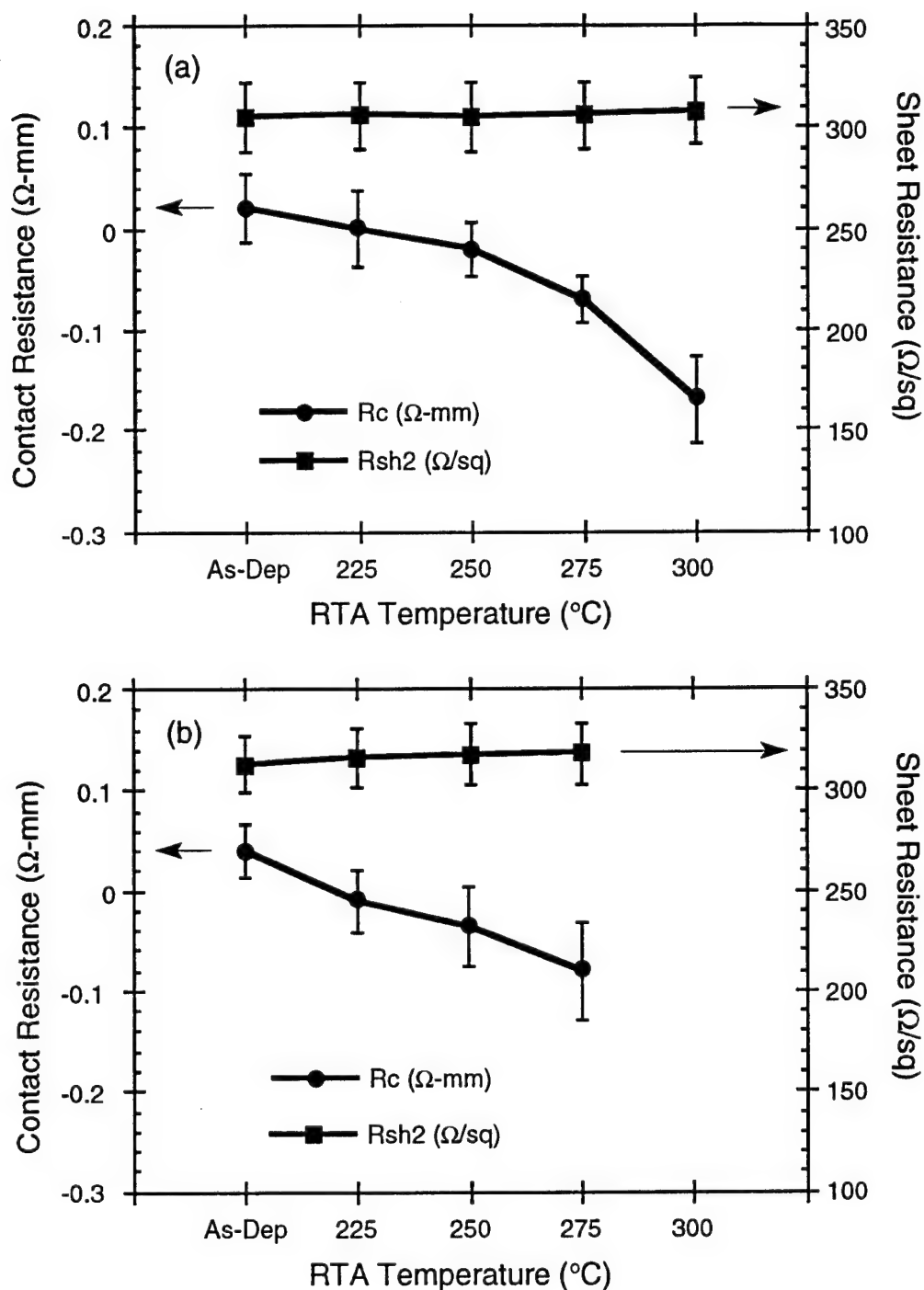


Figure 6.3. Contact resistance (R_c , $\Omega\text{-mm}$) and sheet resistance (R_{sh2} , Ω/sq) for Au/Zn/Au (50/200/3000 \AA) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ as a function of RTA temperature. Sequential annealing was performed on the two samples for (a) 30 seconds, and (b) 5 seconds. TLM measurements were taken at room temperature.

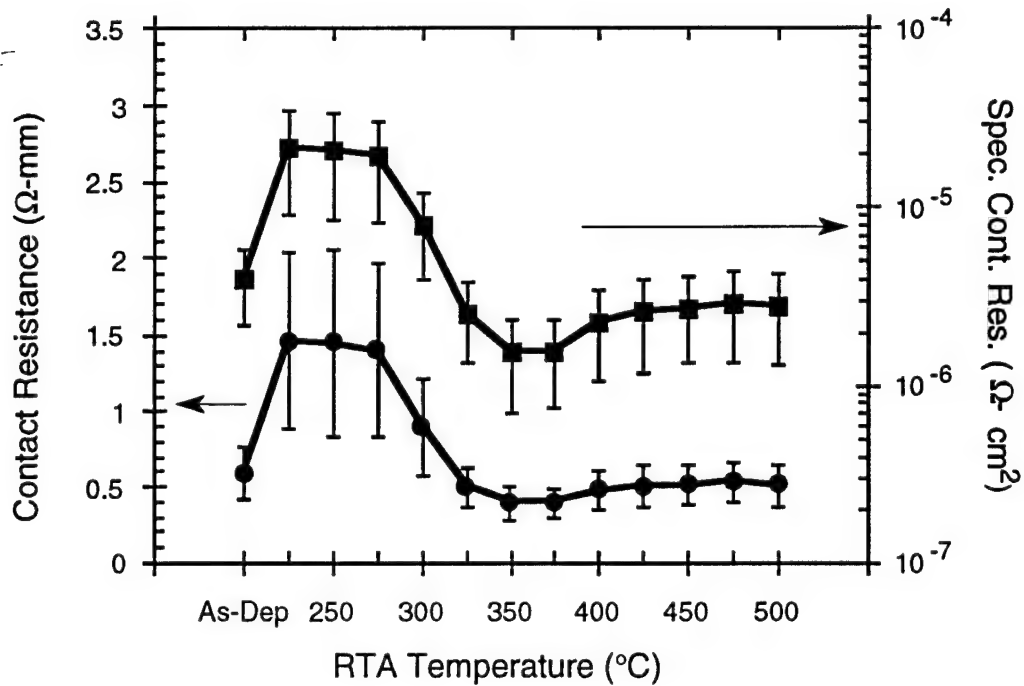


Figure 6.4. Contact resistance (R_c , Ω -mm) and specific contact resistance (ρ_c , Ω -cm²) for Au/Zn/Au (50/100/3000 Å) on MBE-grown GaAs:Be as a function of RTA temperature. Sequential annealing was performed on the sample for 30 seconds at each temperature. TLM measurements were taken at room temperature.

plots extrapolated to negative contact resistance values. No laterally diffusing surface layer was evidenced at any temperature. The low contact resistance, wide RTA temperature window and good surface morphology on the GaAs:Be sample indicate the basic fabrication, evaporation and RTA processes for Au/Zn/Au are of sufficient quality.

Figures 6.5(a) and 6.5(b) present TLM results for Be-implanted, GaAs_{0.51}Sb_{0.49} with a 100 Å Zn layer. The results are similar to those previously obtained for the 200 Å Zn layer. Figure 6.5(a) shows a low, as-deposited specific contact resistance; $\rho_c = 4.6 \times 10^{-7} \Omega$ -cm². The average contact resistance remained close to the as-deposited value following RTA at $T = 225^\circ\text{C}$ and 250°C for 30 seconds. A change in the surface coloration of the Au/Zn/Au towards a grey-gold luster was similarly observed after RTA at 250°C . The laterally diffusing surface layer was detected following the 275°C anneal.

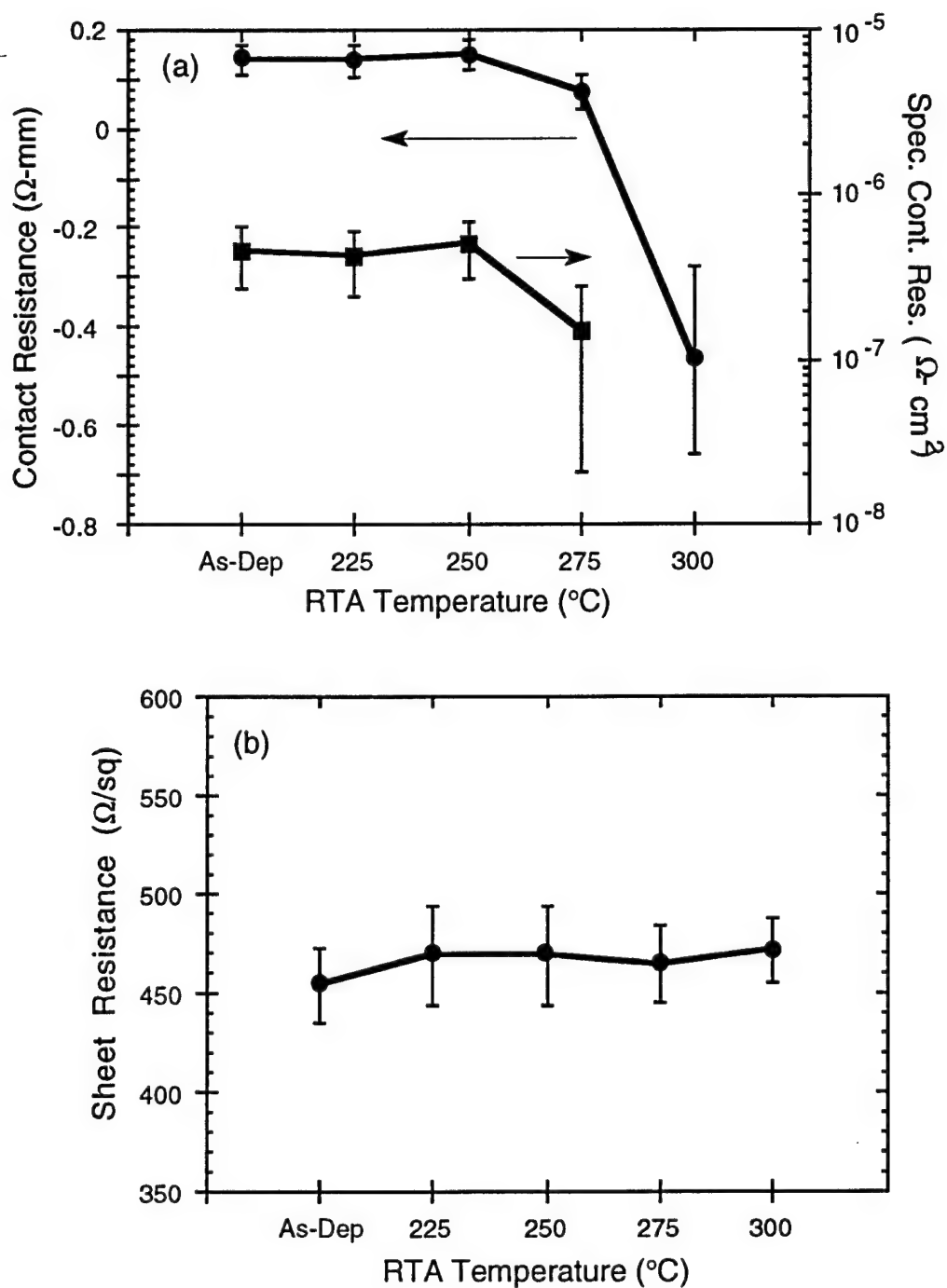


Figure 6.5. TLM results for Au/Zn/Au (50/100/3000 Å) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ as a function of RTA temperature: (a) contact resistance (R_c , $\Omega\text{-mm}$) and specific contact resistance (ρ_c , $\Omega\text{-cm}^2$), and (b) sheet resistance (R_{sh2} , Ω/square). A Be implant dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ was used. Sequential annealing was performed on the sample for 30 seconds at each temperature. TLM measurements were taken at room temperature.

The diffusive surface layer again caused a drastic reduction in R_c as it spread between the contacts as the RTA temperature was raised to 300 °C. Surface diffusion caused electrical shorting between the contacts during RTA at 325 °C. The sheet resistance was again fairly constant over the annealing temperature range as shown in Figure 6.5(b). The TLM measurements show the reduction in Zn thickness to 100 Å still produced low contact resistance values but did not eliminate the lateral surface diffusion. These results demonstrate that lateral surface diffusion consistently causes measurement of negative R_c values following RTA at $T \geq 275$ °C. Measurement of negative resistances following deposition, as in Figure 6.3(a), implies the reaction may initiate at temperatures much less than 275 °C. The insensitivity of the lateral diffusion to Zn layer thickness indicates the diffusive surface layer is most likely unrelated to Zn. The results dictate source (3) is the dominant source of error in TLM measurements of the Au/Zn/Au contact on $\text{GaAs}_{1-x}\text{Sb}_x$.

This series of TLM measurements on the Au/Zn/Au contact indicate a fundamental, degradatory reaction takes place at RTA temperatures as low as $250 \leq T \leq 275$ °C. This reaction renders the Au/Zn/Au contact unsuitable for application in devices using $\text{GaAs}_{1-x}\text{Sb}_x$ as a contact layer. Further studies of the Au/Zn/Au contact with respect to contact stability under long term thermal storage conditions were thus deemed unnecessary. The remaining experimental effort was directed towards identifying the degradation source(s) at the Au/Zn/Au- $\text{GaAs}_{1-x}\text{Sb}_x$ interface.

6.3.2 TLM Thermal Measurements on the Au/Zn/Au Ohmic Contact. Approaching the metal-semiconductor interface as an atomically abrupt junction with uniform material properties is a simplistic approach at best. Complex phases with varying resistivities and geometrical constructions may form on both sides of the junction following thermal cycling, and even during metal deposition. Also, defects may be prevalent as a result of the semiconductor growth, ion implantation and contact annealing. Accurate prediction of the contact resistance prior to measurement is nearly impossible due to these factors.

However, measuring contact resistance under varying ambient temperature yields information concerning hole transport mechanisms across the metal-semiconductor junction. Specifically, determination of the interfacial hole barrier height (ϕ_{BP}) and the fraction of contact area dedicated to field emission (A_f) is possible [11-13]. The barrier height and field emission area are obtained by dissecting the contact into areas of thermionic emission and field emission. These regions are then treated as parallel resistance regions.

In the simplest case, a single emission type is predominant over the entire contact area. If thermionic emission is the only emission type, the specific contact resistance is expressed as [14]

$$\rho_{cth} = \frac{k}{qA^{**}T} \exp\left(\frac{\phi_{BP}}{kT}\right) \quad (6.1)$$

where A^{**} is the “effective” Richardson constant. The effective Richardson constant incorporates perturbations due to phonon scattering and quantum mechanical reflections of the hole by the potential barrier at the metal-semiconductor junction [14,15]. The effective Richardson constant is related to the Richardson constant (A^*) in the following manner:

$$A^{**} = \frac{A^* f_p f_q}{1 + f_p f_q \left(\frac{v_{th}}{v_d}\right)} \quad (6.2)$$

The quantity, f_p , is the probability of hole emission across the potential barrier maximum. Emission probability is decreased when holes are backscattered by optical phonons. The quantity, f_q , is the ratio of the thermionic current to the total current (including quantum mechanical tunneling and reflection). The quantity, v_{th} , is the thermal velocity associated with the transport of holes over the potential barrier. The diffusion velocity, v_d , describes the movement of holes from the depletion region edge in the semiconductor to the barrier

height maximum. In the case of thermionic emission, $v_{th} \ll v_d$ and $f_q = 1$. Additionally, an ideal interface produces $f_p = 1$. Therefore, for an ideal, thermionic interface, $A^{**} = A^*$ (the Richardson constant).

A simple manipulation of Equation (6.1) permits a linear expression of $\ln(\rho_{cth}T)$, with respect to $1/T$.

$$\ln(\rho_{cth}T) = \ln\left(\frac{k}{qA^{**}}\right) + \frac{\phi_{Bp}}{kT} \quad (6.3)$$

Therefore, a linear relationship between $\ln(\rho_c T)$ and $1/T$ indicates thermionic emission dominates across the metal-semiconductor junction. Additionally, ϕ_{Bp} and A^{**} are obtained from a least squares fit of the experimental data to Equation 6.3.

The specific contact resistance was measured under varying ambient temperature for Au/Zn/Au ohmic contacts on Be-implanted GaAs_{0.51}Sb_{0.49}. TLM measurements were made using a Hewlett Packard 4145B Semiconductor Parameter Analyzer and a MMR Technologies LMTP4 thermal probe station with a temperature range of 70 K to 300 °C. Six TLM patterns were measured at each temperature, and the specific contact resistance averaged.

Measurements of ρ_c were taken on the same TLM patterns following Au/Zn/Au deposition and after RTA at $T = 250$ °C for 30 seconds. The resultant plot of $\ln(\rho_c T)$ versus $1/T$ is depicted in Figure 6.6. The as-deposited data points were linear with respect to $1/T$. A least squares fit to the data using Equation 6.3 produced $\phi_{Bp} = 0.021$ eV and $A^{**} = 3.71$ A/(K²·cm²). Thus a very small barrier height was detected in the as-deposited contact. This result indicates the as-deposited sample relies solely on thermionic emission for hole transport across the metal-semiconductor junction. Following RTA at 250 °C the contact no longer demonstrated an Arrhenius behavior, indicating hole transport across the junction was no longer strictly thermionic. Consequently, Equation 6.3 was not

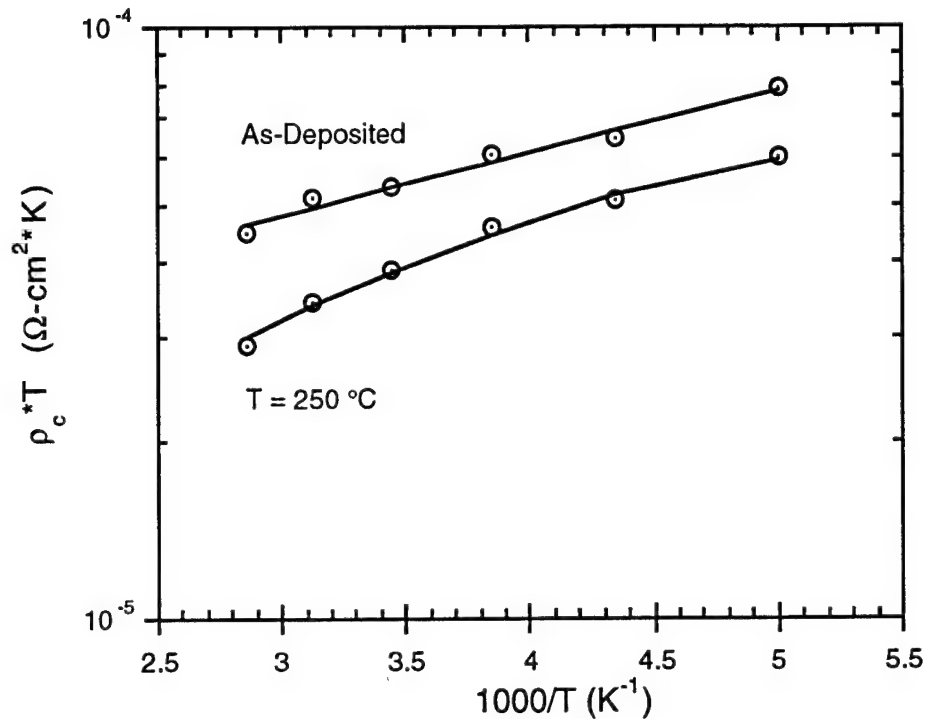


Figure 6.6. The product of specific contact resistance and temperature versus the reciprocal of ambient measurement temperature for Au/Zn/Au (50/100/3000 Å) on Be-implanted GaAs_{0.51}Sb_{0.49}. The data points represent average, measured values of ρ_c . The two data sets are for the as-deposited case and following RTA at $T = 250$ °C for 30 seconds.

employable. Another approach was employed to characterize the barrier height and other properties of the contact as subsequently explained.

Rapid thermal processing tends to produce a metal-semiconductor contact which has regions of either thermionic or field emission [11-13]. This is particularly true in the case of metal contacts applied to highly doped semiconductor layers. Initially, surface contamination, defects or oxides may produce a thermionic contact following metal deposition. Sintering the contact metal through a residual surface layer typically produces a nonuniform, two region contact. The two regions may be treated electrically as parallel resistance regions. The total specific contact resistance is then described by [11]

$$\rho_c = \left(\frac{A_f}{\rho_{cf}} + \frac{1-A_f}{\rho_{cth}} \right)^{-1} \quad (6.4)$$

where ρ_{cf} is the specific contact resistance of the field emission region of the contact. Determination of A_f and ρ_{cf} for the Au/Zn/Au contact was achieved through: (1) substitution of Equation 6.1 into 6.4 followed by, (2) a least squares fit of Equation 6.4 to the ρ_c versus T experimental data, allowing ϕ_{BP} , A^{**} , ρ_{cf} and A_f to vary.

Figure 6.7 demonstrates ρ_c as a function of ambient temperature for Au/Zn/Au (50/100/3000 Å) on Be-implanted GaAs_{0.51}Sb_{0.49}. A continuous reduction in ρ_c was observed over the entire measurement temperature range. Also, ρ_c following annealing was consistently below that of the as-deposited values. The specific contact resistance dropped following RTA at $T = 250$ °C and remained below the as-deposited values over the entire measurement temperature range. Least square fits to the experimental data are depicted by solid curves. The least squares fit for the $T = 250$ °C sample was accomplished using equation 6.4. Fitted values of $\rho_{cf} = 5.51 \times 10^{-8} \Omega\text{-cm}^2$, $A_f = 0.10$, $A^{**} = 15.2 \text{ A}/(\text{K}^2\text{cm}^2)$ and $\phi_{BP} = 0.052 \text{ eV}$ were obtained. Thus considerable changes in the electrical composition of the contact occurred during RTA. A tunneling region with a specific contact resistance of $5.51 \times 10^{-8} \Omega\text{-cm}^2$ was created and comprises 10 % of the contact area. The thermionic emission characteristics had changed as indicated by the increase in ϕ_{BP} from 0.021 to 0.052 eV and the increase in A^{**} . The fact that ρ_c decreases even though the barrier height of the thermionic region increases, indicates the majority of the hole transport through the contact occurs in the small area, field emission region. The increases in both ϕ_{BP} and A^{**} at the low RTA temperature of $T = 250$ °C implies the Au/Zn/Au contact is thermally unstable on Be-implanted GaAs_{0.51}Sb_{0.49}. In similar studies of p-type ohmic contacts to GaAs [12], In_{0.53}Ga_{0.47}As [11] and InAs [13] the barrier height of the thermionic region remained constant following RTA.

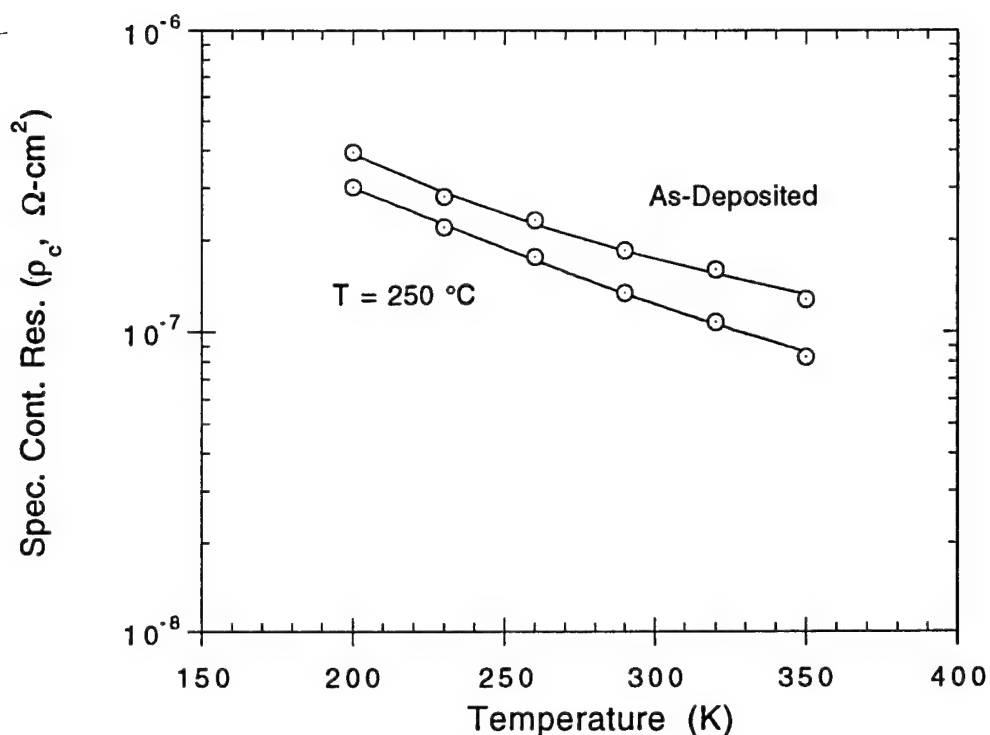


Figure 6.7. Specific contact resistance versus the ambient measurement temperature for Au/Zn/Au (50/100/3000 Å) on Be-implanted GaAs_{0.51}Sb_{0.49}. The data points represent average, measured values of ρ_c while solid curves represent a least squares fit. The two data sets are for the as-deposited case and following RTA at T = 250 °C for 30 seconds.

6.3.3 Hall Effect Thermal Measurements. Additional temperature dependent, electrical measurements were made on Be-implanted GaAs_{0.51}Sb_{0.49}. These results, supplemented with Hall effect measurements, provide insight on the electrical properties of Be-implanted GaAs_{0.51}Sb_{0.49} under varying ambient temperature conditions.* All TLM and Hall effect measurements referenced in this section were obtained on Be-implanted

* Experimental sheet resistance results were obtained from TLM measurements using the thermal probe station and Au/Zn/Au contacts. Therefore, sheet resistance results on Be-implanted GaAs_{0.51}Sb_{0.49} are included in this section as opposed to Chapter V. Hall effect measurements and analysis are also included in this section to allow direct comparison of sheet resistance measurements taken using Hall and thermal probe techniques.

GaAs_{0.51}Sb_{0.49}/InP with implant parameters: $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, $E = 50 \text{ keV}$ and $\theta = 7^\circ$, and RTA parameters: $T = 600^\circ \text{C}$ for 10 seconds.

Current versus voltage results are presented in Figure 6.8 for as-deposited Au/Zn/Au (50/100/3000 Å). The I-V characteristics were taken across the largest TLM gap ($L = 21 \mu\text{m}$) and are presented for three ambient temperatures, $T = 200, 290$ and 350 K . The decreasing slope implies resistance increased with an increase in the ambient temperature. The total resistance consists of the series resistance of two Au/Zn/Au contact resistances and the GaAs_{0.51}Sb_{0.49} resistance. Since the total resistance increased with temperature while the contact resistance decreased, the sheet resistance of the GaAs_{0.51}Sb_{0.49} must increase over this temperature range.

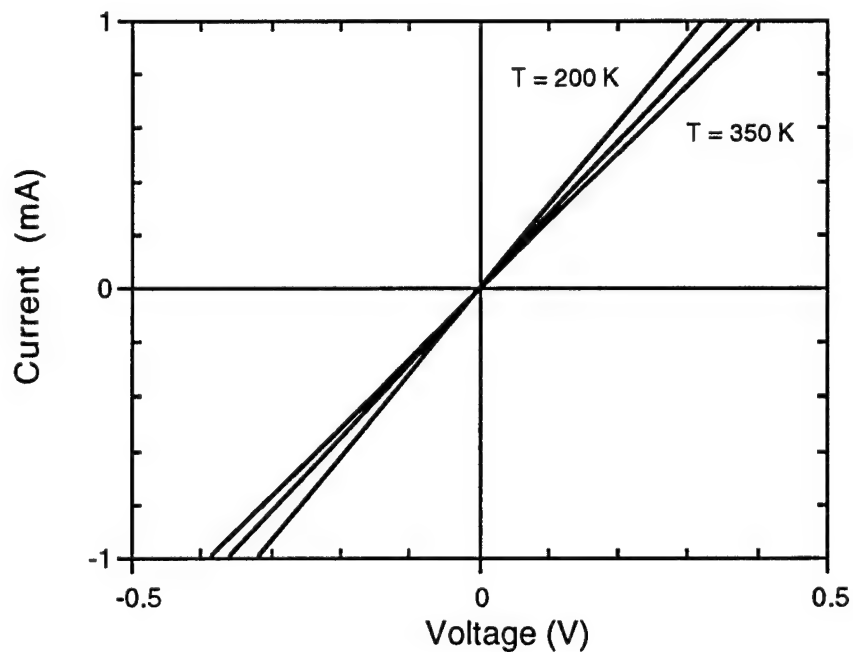


Figure 6.8. Current versus voltage measurements taken across the largest TLM gap ($L = 21 \mu\text{m}$) for as-deposited Au/Zn/Au (50/100/3000 Å) on Be-implanted GaAs_{0.51}Sb_{0.49}. Measurements for three ambient temperatures are shown: $T = 200, 290$ and 350 K .

An increase in the sheet resistance of the Be-implanted GaAs_{0.51}Sb_{0.49} with increasing temperature was verified by both TLM and Hall effect measurements. Figure 6.9 demonstrates the sheet resistance, R_{sh2} , as a function of ambient measurement temperature. The results were obtained by measuring R_{sh2} on as-deposited, Au/Zn/Au TLM patterns, and using Hall effect. (Hall measurements were taken on a 4 x 4 mm² sample with a magnetic field of 5 kG and a current of 5 mA.) The sheet resistance results measured by the two methods are very close in value and have the same trend with respect to temperature - a continuous increase in R_{sh2} . Accordingly, consistency between the TLM and Hall measurements was realized. The continuous increase in R_{sh2} over the temperature range $100 \leq T \leq 400$ K explains the inverse relationship between the total resistance and contact resistance. Also shown in the figure is the hole sheet concentration, p_s , obtained by Hall measurement. The hole sheet concentration was essentially constant over the measurement temperature range with $p_s \approx 4.7 \times 10^{14} \text{ cm}^{-2}$. The constancy of p_s indicated the implanted Be is fully ionized. The high acceptor density obtained by implantation implies that p_s is dominated by the sheet acceptor density, ($p_s = N_{AS}$) over this temperature range. The magnitude of N_{AS} also demonstrated a high implant activation percentage since $N_{AS}/Q_0 = 0.94$.

Sheet resistivity, R_{sh2} , in a p-type semiconductor is controlled by the hole density and hole mobility. Sheet resistivity in a highly doped, p-type semiconductor is expressible in terms of quantities obtained through Hall effect measurements

$$R_{sh2} = \frac{\rho}{t} = \frac{1}{q\mu_p t} \equiv \frac{1}{q\mu_H N_{AS}} \quad (6.5)$$

where ρ is the resistivity, t is the active layer thickness, and μ_H is the measured Hall mobility. The experimental results of Figure 6.9 demonstrated an increase in R_{sh2} and a constant hole sheet concentration as the temperature was increased. These trends in R_{sh2}

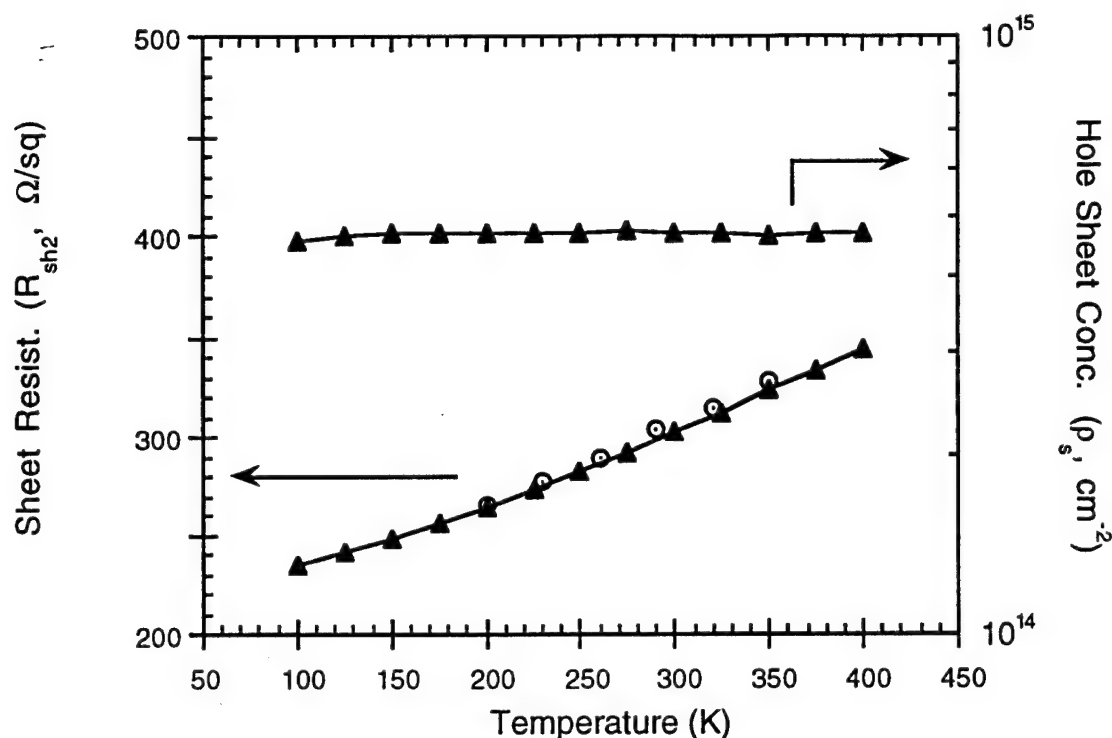


Figure 6.9. Sheet resistance and hole sheet concentration versus ambient measurement temperature on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The data was obtained using either Hall effect measurements (closed, connected triangles) on a bulk sample or TLM measurements (dotted, unconnected circles) on as-deposited Au/Zn/Au (50/100/3000 Å).

and N_{AS} with temperature dictate a decrease in mobility based upon Equation 6.5. Mechanisms causing a decrease in mobility with increasing temperature were subsequently investigated using phenomenological modeling of μ_H with respect to ambient measurement temperature.

Numerous mechanisms may contribute to mobility reduction in a III-V semiconductor as the temperature is raised. Principally, mobility is reduced by scattering a carrier from it's forward path. Scattering is produced by localized defects, lattice interactions and other carriers [16]. In GaAs the predominant scattering mechanisms are ionized impurity scattering at low temperature ($T < 50$ K), acoustic phonon scattering due to the deformation potential at $50 \leq T \leq 100$ K, and polar optical phonon scattering at

higher temperatures ($100 < T \leq 300$ K) [17]. Alloy scattering produces an additional scattering source in ternary semiconductors. Alloy scattering effects were observed in MBE grown, p-type $\text{Al}_x\text{Ga}_{1-x}\text{As}$ [18] and theoretically investigated in p-type $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ [19]. The low hole mobility measured in nominally undoped, near-lattice-matched $\text{GaAs}_{1-x}\text{Sb}_x$ has been attributed to alloy scattering [20] and compositional clustering [21]. The mobility is further reduced by high acceptor doping. For example, $29 < \mu_H < 44$ $\text{cm}^2/\text{V}\cdot\text{s}$ when $2 \times 10^{19} \leq N_A \leq 4 \times 10^{19} \text{ cm}^{-3}$ in $\text{GaAs}_{0.51}\text{Sb}_{0.49}:\text{Be}$ [22] at $T = 300$ K. Consequently, investigating the effect of scattering mechanisms on the experimental hole mobility in Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ is warranted.

The remainder of this section is dedicated to describing predominant hole scattering mechanisms and modeling the temperature dependence of the hole mobility in Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The mobility of Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ was measured with respect to ambient temperature. The mobilities associated with predominant scattering mechanisms for degenerately doped, p-type $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ are subsequently calculated and compared against the measured mobility. A brief explanation of each mechanism and the corresponding mobility are first presented.

In the case of electron mobility in n-type, III-V semiconductors, the temperature dependence of the mobility is readily modeled using closed form expressions for each scattering mobility component and Matthiessen's rule. Matthiessen's rule is expressed [16]

$$\mu = \sum_{i=1}^m \left(\frac{1}{\mu_i} \right)^{-1} \quad (6.5b)$$

where the μ_i are the mobility contributions from each of the m scattering mechanisms. The closed form approach for electron mobility is valid due to the s-like wave functions of the electrons, the spherically symmetric dispersion relation (E vs k) of the conduction band and the nondegenerate electron energy levels [23]. The situation for p-type mobility modeling

in III-V semiconductors is more complex since, the hole wave functions have p-like symmetry, the light and heavy hole bands are degenerate at the zone center, and the dispersion relation is anisotropic.

A rigorous approach for theoretically determining p-type mobility involves numerical solution of two, coupled Boltzmann transport equations. Solution of the Boltzmann equations requires knowledge of the dispersion relation for the $\text{GaAs}_{1-x}\text{Sb}_x$ hole bands - a nontrivial theoretical effort [23,24]. Another approach phenomenologically addresses the issues of degenerate bands, anisotropic dispersion and p-like hole wave functions. This approach modifies the closed form expressions used for n-type mobility calculations. In particular, the effective mass is mathematically presented as a mixture of the light and heavy hole effective masses. Closed form, approximate expressions for the p-type semiconductor are thus realized. The phenomenological approach permits study of the gross impact of different scattering mechanisms on the mobility of Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The phenomenological mobility expressions due to ionized impurity scattering, alloy scattering, polar optical phonon scattering and nonpolar optical phonon scattering are next provided.

Ionized impurity scattering occurs due to the screened Coulombic potential encountered by a carrier as it passes near an impurity site. A strong $T^{3/2}$ dependence is exerted on the mobility by ionized impurities in the nondegenerate case at low temperatures. In a degenerate semiconductor, the effect on mobility due to ionized impurity scattering is temperature independent. The degenerate ionized impurity scattering mobility, μ_{iid} , is derived from the Brooks-Herring formalism [16,23] and is expressed as

$$\mu_{iid} = Q \frac{r^{1/2} + r^{3/2}}{1 + r^{3/2}} \cdot \frac{3\epsilon_s^2 h^3 p}{N_I Z^2 q^3 m_{hh}^* \left[\ln(1+y_F) - \left(\frac{y_F}{1+y_F} \right) \right]} \quad (6.6a)$$

where

$$y_F = \frac{3^{1/3} \pi^{2/3} \epsilon_s \hbar^2 p^{1/3}}{q^2 m_{hh}^*} \quad (6.6b)$$

and Zq is the ionic charge, N_I is the ionized impurity density, p is the hole density, and $r = m_{hh}^*/m_{lh}^*$. The factor, Q , accounts for the p-like symmetry of the hole wave functions ($1 \leq Q \leq 2$). In the case of highly doped, Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ a singly ionized impurity exists with a completely ionized acceptor density when $T \geq 100$ K as per Figure 6.9. Therefore $Z = 1$ and $p = N_I = N_A \equiv 2.5 \times 10^{19} \text{ cm}^{-3}$ (as derived from the Polaron results of Figure 5.13). The factor Q is chosen as $Q = 1.5$.

Alloy scattering is another mechanism which impedes carrier transport in ternary semiconductors such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and $\text{GaAs}_{1-x}\text{Sb}_x$. In $\text{GaAs}_{1-x}\text{Sb}_x$ a carrier may travel from a localized region which has Ga and As nearest neighbors to a region which has Ga and Sb nearest neighbors. Thus the carrier experiences a varying localized potential as it traverses the lattice. The probability of alloy scattering maximizes when the atomic percentages of group III or V alloys are equal, $x = 1-x$. Such a condition occurs in $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The mobility associated with alloy scattering, μ_{al} , is expressed as [16]

$$\mu_{al} = \frac{1}{2^{5/2} 3 \pi^{7/2}} \frac{q \hbar^4}{V_c x(1-x) \Delta E_V^2 (m_{hh}^{*3/2} + m_{lh}^{*3/2})^{5/3} (kT)^{1/2}} \quad (6.7)$$

where V_c is the primitive cell volume, x is the Sb atomic percentage, and ΔE_V is the valence band discontinuity between GaAs and GaSb. For $\text{GaAs}_{0.51}\text{Sb}_{0.49}$, $V_c = 5.06 \times 10^{-29} \text{ m}^3$, and $\Delta E_V = 0.9 \text{ eV}$ [25]. The parenthetical expression containing the effective masses employs the density of states hole effective mass [17]. Most notably, the alloy scattering mobility exhibits a $T^{-1/2}$ dependence. Other scattering mechanisms due to localized

potentials vary as $T^{-1/2}$, including potential barriers and wells, and space charge regions [16]. Separating each mechanism by temperature dependence alone is not feasible. However, in the case of lattice matched $\text{GaAs}_{0.51}\text{Sb}_{0.49}$, where the alloy nature of the lattice is greatest for $\text{GaAs}_{1-x}\text{Sb}_x$, a reasonable assumption is dominance of alloy scattering for mechanisms with a $T^{-1/2}$ dependence [24].

Polar optical phonon scattering occurs in semiconductors with a partially ionic nature such as GaAs. Optical phonons interact with the sublattices and subsequently induce a long range Coulombic force through the creation of dipole moments. The polar optical phonon mobility, μ_{po} , is expressed by [16,23]

$$\mu_{po} = 2K \cdot \frac{2^{5/2}}{3\pi^{3/2}} \frac{h^2(kT)^{1/2}(\exp(T_{po}/T)-1)\chi(T_{po}/T)}{qkT_{po}m_{hh}^{*3/2}(\epsilon_{s\infty}^{-1}-\epsilon_s^{-1})} \quad (6.8a)$$

where

$$\chi(T_{po}/T) = 1 - 0.5841(T_{po}/T) + 0.2920(T_{po}/T)^2 - 0.037164(T_{po}/T)^3 + 0.0012016(T_{po}/T)^4 \quad (6.8b)$$

The factor 2 accounts for the p-like symmetry of the hole wave functions. T_{po} is the polar optical phonon Debye temperature and $\epsilon_{s\infty}$ is the high frequency dielectric permittivity. The quantities $T_{po} = 383$ K [26], $\epsilon_{s\infty} = 12.7$ [27], and $\epsilon_s = 14.4$ [27] when linear interpolation between the GaAs and GaSb endpoint binary semiconductors is employed. K is a tabulated correction factor which accounts for the light hole contribution to the mobility (using linear interpolation, $K = 1.15$ for $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ [23]).

Acoustic mode phonons produce changes in the lattice spacing, inducing point-to-point variations in the bandgap energy. The change in bandgap energy is viewed as a

"deformation potential". The mobility due to deformation potential scattering, μ_{dp} , is represented as [16,23]

$$\mu_{dp} = \frac{r^{5/2}(1 + r^{1/2})}{(1 + r^{3/2})^2} \frac{\sqrt{8\pi} q h^4 C_1(x)}{3E_{ac}^2 m_{hh}^{*5/2} (kT)^{3/2}} \quad (6.9)$$

Clearly, μ_{dp} has a $T^{-3/2}$ dependence. E_{ac} is the phenomenological valence band deformation potential for $\text{GaAs}_{1-x}\text{Sb}_x$ expressed by [27]

$$E_{ac} = \sqrt{\frac{\gamma + 2}{6\gamma}} E_{eff} \quad (6.10)$$

where the ratio of the transverse and longitudinal elastic constant is given by $\gamma = C_t(x)/C_l(x)$, and E_{eff} is the effective valence band deformation potential. The elastic constants are [27]

$$C_l(x) = \frac{1}{5}[3C_{11}(x) + 2C_{12}(x) + 4C_{44}(x)] \quad (6.11a)$$

$$C_t(x) = \frac{1}{5}[C_{11}(x) - C_{12}(x) + 3C_{44}(x)] \quad (6.11b)$$

where the $C_{ij}(x)$ are the bulk elastic constants with respect to Sb composition. E_{eff} is given by [27]

$$E_{eff} = \left[a(x)^2 + \gamma^2 \left(b(x)^2 + \frac{d(x)^2}{2} \right) \right]^{1/2} \quad (6.12)$$

where $a(x)$, $b(x)$ and $d(x)$ are the valence band deformation potentials for $\text{GaAs}_{1-x}\text{Sb}_x$. Values subsequently used for $C_{ij}(x)$, $a(x)$, $b(x)$ and $d(x)$ were obtained through linear

interpolation between the GaAs and GaSb values cited in References 27 and 22, respectively. Linear interpolation yields (in N/m²): $C_{11} = 1.04 \times 10^{11}$, $C_{12} = 4.72 \times 10^{10}$, $C_{44} = 5.19 \times 10^{10}$, $C_1 = 1.23 \times 10^{11}$, $C_t = 4.25 \times 10^{10}$; and (in eV) $a = 8.92$, $b = -2.49$, $d = -6.34$, $E_{\text{eff}} = 12.47$ and $E_{\text{ac}} = 13.25$.

Figure 6.10 illustrates: (i) individual, calculated scattering mobilities μ_{iid} , μ_{al} , μ_{po} and μ_{dp} , (2) the experimentally measured Hall mobility, μ_{H} , and (3) a least squares fit to μ_{H} using Matthiessen's rule. The individual theoretical scattering mobilities were calculated using previously described equations and physical values. Heavy hole and light hole effective masses for GaAs_{0.51}Sb_{0.49} are required for calculating each scattering mobility. The effective masses were obtained through linear interpolation: $m_{\text{hh}}^*/m_0^* = 0.53$ (GaAs[28],GaSb[29]) and $m_{\text{lh}}^*/m_0^* = 0.061$ (GaAs[28],GaSb[27]). The experimental Hall mobility was measured on the Be-implanted, GaAs_{0.51}Sb_{0.49} sample used in Figure 6.9.

A few observations related to the individual, theoretical mobilities are apparent from the Figure 6.10. All of the theoretical scattering mobilities except μ_{iid} decreased over the temperature range. Also, each of the theoretical mobilities were greater than 90 cm²/V·s. A comparison of the theoretical mobilities indicates alloy scattering is the predominant mechanism for reducing hole mobility at temperatures $100 \leq T \leq 400$ K. Ionized impurities produce the second most predominant theoretical scattering for $T < 280$ K while μ_{dp} dominates μ_{iid} for $T > 280$ K. Polar optical phonon scattering plays a very minor role in mobility reduction since $\mu_{\text{po}} \geq 900$ cm²/V·s over the entire temperature range.

The experimental Hall mobility also provoked observations. A continuous decrease in μ_{H} occurred as T increased. This mobility decrease correlates with the experimental measurements of Figure 6.9 which demonstrated an increase in R_{sh2} over the same temperature range. The logarithm of the experimental mobility was nearly linear with a very low temperature dependence. The hole mobility limits were $38 \leq \mu_{\text{H}} \leq 64$ cm²/V·s

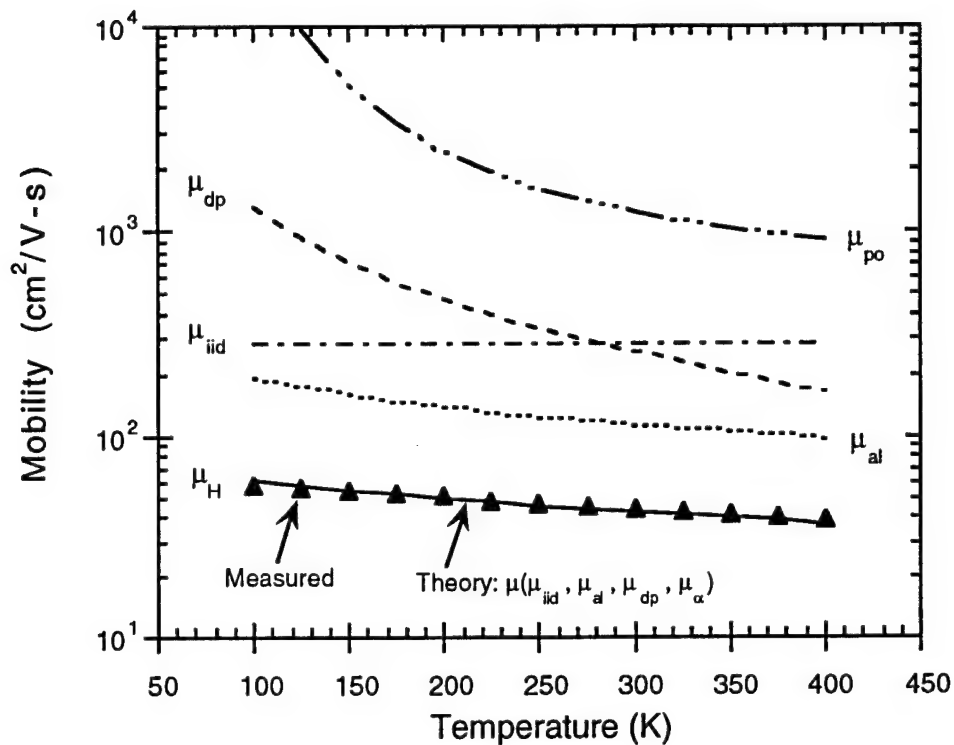


Figure 6.10. Theoretical scattering mobilities and experimental Hall mobility (μ_H) versus ambient temperature on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. Shown are theoretical mobility values for the following scattering mechanisms: ionized impurity scattering (μ_{iid}), alloy scattering (μ_{al}), acoustic mode phonon scattering (deformation potential) (μ_{dp}), and polar optical phonon scattering (μ_{po}). Measured μ_H values are shown as closed triangles. A least squares, theoretical fit to the measured μ_H values was obtained by application of Matthiessen's rule using μ_{iid} , μ_{al} , μ_{dp} , and an additional, temperature independent, scattering mobility $\mu_{\alpha} = 143 \text{ cm}^2/\text{V}\cdot\text{s}$.

over the fairly wide temperature range. A least squares fit to μ_H demonstrated a temperature dependence of $T^{-0.29}$. This temperature dependence is far lower than the $T^{-1/2}$ to $T^{-3/2}$ predicted by most theoretical scattering mobilities.

A least squares fit to $\mu_H(T)$ was attempted using theoretical expressions for μ_{iid} , μ_{al} , μ_{po} and μ_{dp} with Matthiessen's rule. Fitting was attempted over all possible single and multiple combinations of the theoretical mobilities. The heavy hole effective mass was allowed to vary during the fitting procedure. A satisfactory fit to the experimental data was

not possible unless: (1) the heavy hole effective mass was increased to $m_{hh}^*/m_0^* = 0.74$ and only μ_{iid} and μ_{al} were applied or (2) a temperature independent scattering mobility, μ_{α} , was included in Matthiessen's rule. Using $\mu_{\alpha} = 143 \text{ cm}^2/\text{V}\cdot\text{s}$ the least squares fit shown in Figure 6.10 was obtained through inclusion of μ_{iid} , μ_{al} , μ_{dp} and μ_{α} , in Matthiessen's rule. These results demonstrate that the hole mobility in Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$ may be impacted by a larger effective hole mass than linear interpolation affords. Furthermore, an additional, temperature independent scattering component may account for the low μ_H and its relative temperature independence. Temperature independent scattering is caused by non-ionized impurities [16] and crystalline inhomogeneities [29]. Application of these scattering mechanisms requires accurate knowledge of non-ionized impurity densities and the volume fraction of inhomogeneities, however. Consequently, additional, in-depth theoretical and experimental studies of the hole mobility in Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$ are warranted to identify all scattering mechanisms.

6.4 Microstructural Characterization of the Au/Zn/Au Ohmic Contact

This section presents microstructural characterization results obtained on as-deposited and annealed Au/Zn/Au (50/200/1000 Å) films on $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. A number of characterization methods were used, to include atomic force microscopy (AFM), Auger electron spectroscopy (AES), X-ray diffraction (XRD), cross-section transmission electron microscopy (XTEM), selected area diffraction (SAD) and energy dispersive X-ray analysis (EDX).

The samples used in each characterization method originated from the same, 2" diameter, (100) InP:Fe wafer. The $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ epilayer thickness was 1 μm . The Be ion implantation and anneal procedure were performed as previously described in Section 5.3 (implant: $E = 50 \text{ keV}$, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$; RTA: $T = 600 \text{ }^\circ\text{C}$, $t = 10 \text{ seconds}$). The Au surface layer was reduced to 1000 Å thick as opposed to the 3000 Å thick layer used on

TLM samples. Gold thickness reduction was warranted in order to facilitate XRD and AES which require penetration of this layer. Samples of Au/Zn/Au on GaAs_{0.51}Sb_{0.49} were evaluated following metal deposition or after RTA at $T = 250^\circ$ or 325°C for 30 seconds. These RTA temperatures were selected based upon the results of Figure 6.2. The three samples represent the initial metal-semiconductor construction, the RTA temperature which minimizes R_c , and the RTA temperature which causes thorough electrical degradation.

6.4.1 Atomic Force Microscopy Results. Atomic force microscopy is a non-destructive characterization technique which permits determination of surface topography to angstrom-level precision [30]. This characterization method is particularly advantageous for the evaluation of metal or semiconductor surfaces [31]. A brief description of the AFM system is now presented.

In contact mode AFM, a Si₃N₄ stylus is attached underneath a cantilever. The stylus is scanned across the sample surface. A laser beam is directed onto the top of the cantilever, and subsequently reflected onto a photodetector. Stylus movement in the z direction deflects the laser spot away from the photodetector. The photodetector is electronically coupled to a feedback system which adjusts the sample stage height to maintain an undeflected spot. The feedback control voltage is proportional to the z deflection of the cantilever. Hence, topographical mapping of surface morphology is possible as the cantilever is scanned in the x and y direction. AFM measurements were taken with a Nanoscope II system (Digital Instruments, Inc., Santa Barbara, CA). The scan area was $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$ unless otherwise depicted. Height measurements were taken at every 1/200 of the maximum x or y scan distance (40,000 individual measurements per scan area).

Atomic force microscopy results are shown in Figures 6.11 and 6.12(a) through 6.12(c). Figure 6.11 is an AFM micrograph of the GaAs_{0.51}Sb_{0.49}/InP sample surface following implantation and RTA. Figures 6.12(a)-6.12(c) show surface micrographs of

Au/Zn/Au samples. Measurements of the corresponding root-mean-square (rms) roughness, peak-to-valley roughness and grain diameter size range are supplied in Table 6.1.

Figure 6.11 demonstrates the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface following implantation and RTA is smooth in relation to the thickness of the metal layers. The aspect ratio of the thinnest Au layer thickness to the rms roughness of the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface is $50/6 = 8.3$. Also, there are no abrupt geometries emanating along the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. Therefore, evaporated metal layers nominally cover the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface.

Considerable variations in the smoothness and geometry of the Au/Zn/Au occur as the RTA temperature is increased (Figure 6.12). The as-deposited surface was composed of ovaline grains which were almost circular from a plan view. Annealing at $T = 250^\circ\text{C}$ smoothed the metal surface and increased the grain size. The rms surface roughness decreased from $\pm 25 \text{ \AA}$ to $\pm 19 \text{ \AA}$ while the pk-val roughness decreased from $\pm 280 \text{ \AA}$ to $\pm 160 \text{ \AA}$. The reduction in roughness and increase in grain size are advantageous from the standpoint of depositing additional interconnect metallizations. RTA at $T = 325^\circ\text{C}$ produced a degradatory effect on the surface smoothness. The rms and pk-val roughness increased approximately seven fold over the $T = 250^\circ\text{C}$ value while the grain diameter increased by a factor of 10. Inspection of Figure 6.12(c) clearly shows grain plateaus extending roughly 400 \AA from minima locations. Coverage of such a surface area would require metal layers at least 500 \AA thickness, approximately. These results demonstrate annealing the Au/Zn/Au contact at $T = 250^\circ\text{C}$ improves surface morphology, while a small increase in RTA temperature to $T = 325$ causes considerable surface roughness.

6.4.2 Auger Electron Spectroscopy Results. Auger electron spectroscopy was conducted on the Au/Zn/Au samples in order to obtain elemental depth profiles. A Perkin-Elmer PHI 660 Scanning Auger Microanalyzer was used. A 10 keV electron beam was used to stimulate Auger transitions from within the samples. Samples were sputtered with

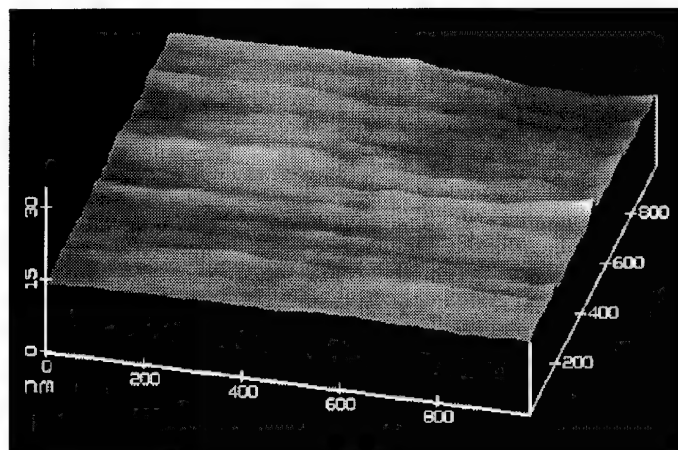
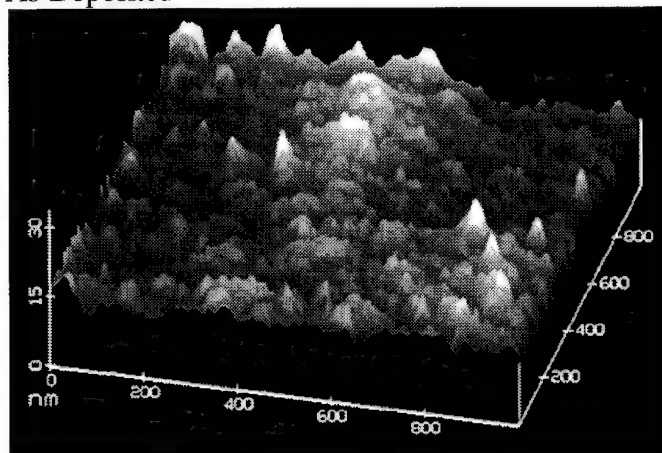


Figure 6.11. Atomic force micrograph of the GaAs_{0.51}Sb_{0.49} surface following Be ion implantation at $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and $E = 50 \text{ keV}$, and RTA at 600°C for 10 seconds. All scales are in nanometers.

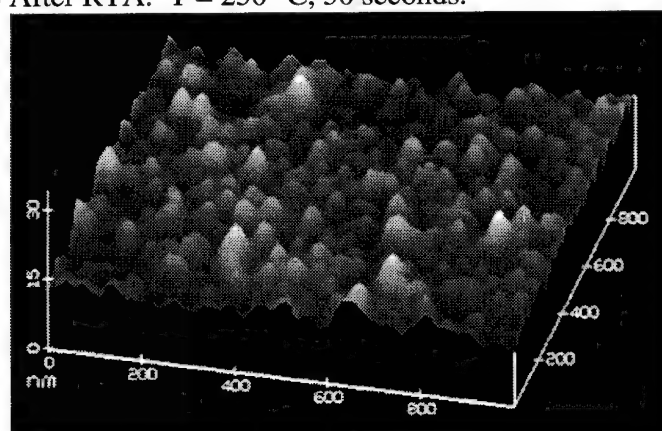
Table 6.1. Summary of Surface Roughness by Atomic Force Microscopy:
Au/Zn/Au on Beryllium-Implanted GaAsSb

Deposition or RTA Condition	RMS Roughness (\AA)	Pk-Val Roughness (\AA)	Grain Dia. (μm)
Post Implant & RTA	± 6	63	N/A
As-Deposited Au/Zn/Au	± 25	280	0.015 - 0.063
250 $^\circ\text{C}$, 30 sec Au/Zn/Au	± 19	160	0.031 - 0.140
325 $^\circ\text{C}$, 30 sec Au/Zn/Au	± 137	1030	0.380 - 1.55

(a) As-Deposited



(b) After RTA: $T = 250\text{ }^{\circ}\text{C}$, 30 seconds.



(c) After RTA: $T = 325\text{ }^{\circ}\text{C}$, 30 seconds.

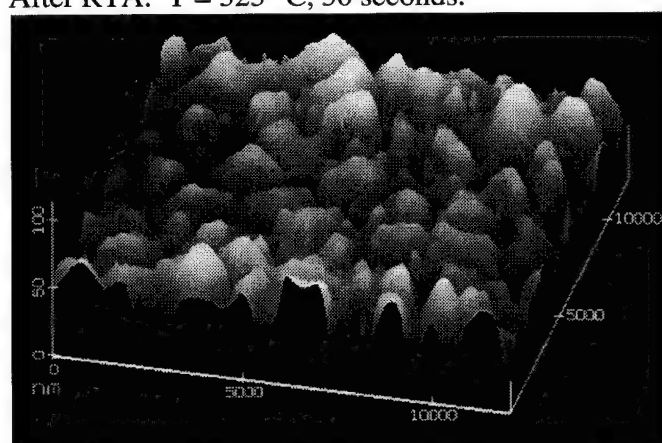


Figure 6.12. Atomic force micrographs of Au/Zn/Au (50/200/1000 Å) surface: (a) as-deposited, and following RTA at (b) 250 °C or (c) 325 °C for 30 seconds. All scales are in nanometers.

a 20 nA, 4 keV Ar⁺ primary ion beam. The ion beam was raster scanned over a 200 μm x 200 μm analysis crater. Auger transitions from Au-MNN (2024 eV), Zn-LLM (994 eV), Ga-LMM (1070 eV), As-LMM (1228 eV), Sb-MNN (454 eV), and O-KLL (510 eV) were monitored in a sputter/analysis mode. The AES data was collected from the center of the crater over an area approximately one-tenth of the total crater area. Figures 6.13(a) through 6.13(f) illustrate the AES depth profiles for the elements Au, Sb, As, Ga, Zn and O.

The metal semiconductor interface was well delineated by a drop off in the as-deposited Au signal. Some Au diffusion may have occurred into the GaAs_{0.51}Sb_{0.49} during deposition as indicated by a tail emerging at a depth of 1400 Å. Subsequent rapid thermal annealing at T = 250 °C and 325 °C causes considerable indiffusion of the Au. Indiffusion is evidenced by Au signal reduction at the surface as the RTA temperature was increased. Gold concentration peaks were obtained at depths of 2700 Å and 7200 Å below the sample surface. No Sb was observed in the Au layer after deposition. However, considerable Sb outdiffusion and surface massing began at T = 250 °C. RTA at T = 325 °C caused further Sb outdiffusion and massing from deep within the GaAs_{0.51}Sb_{0.49}. Little As outdiffusion or surface massing was detected following deposition or RTA. RTA at T = 325 °C resulted in regions of As massing and depletion in the GaAs_{0.51}Sb_{0.49}. No Ga outdiffusion or surface massing were detected following deposition. Gallium outdiffusion occurred at T = 250 °C. RTA at T = 325 °C caused alternating regions of accumulation and depletion with depth. The regions deficient in Ga and As corresponded to Au-rich regions. Zinc detection was limited by interference of the Zn-LLM (994 eV) line with a secondary Ga line. Consequently, Zn profiles were only available at depths less than 1300 Å in the as-deposited and T = 250 °C cases. The as-deposited spectrum shows a Zn peak in the Au surface layer near the Au-GaAs_{0.51}Sb_{0.49} interface. The Zn concentration reduced following RTA at T = 250 °C. A small oxygen signal was detected at the Au-GaAs_{0.51}Sb_{0.49} interface after deposition. The O signal decreased at the interface and

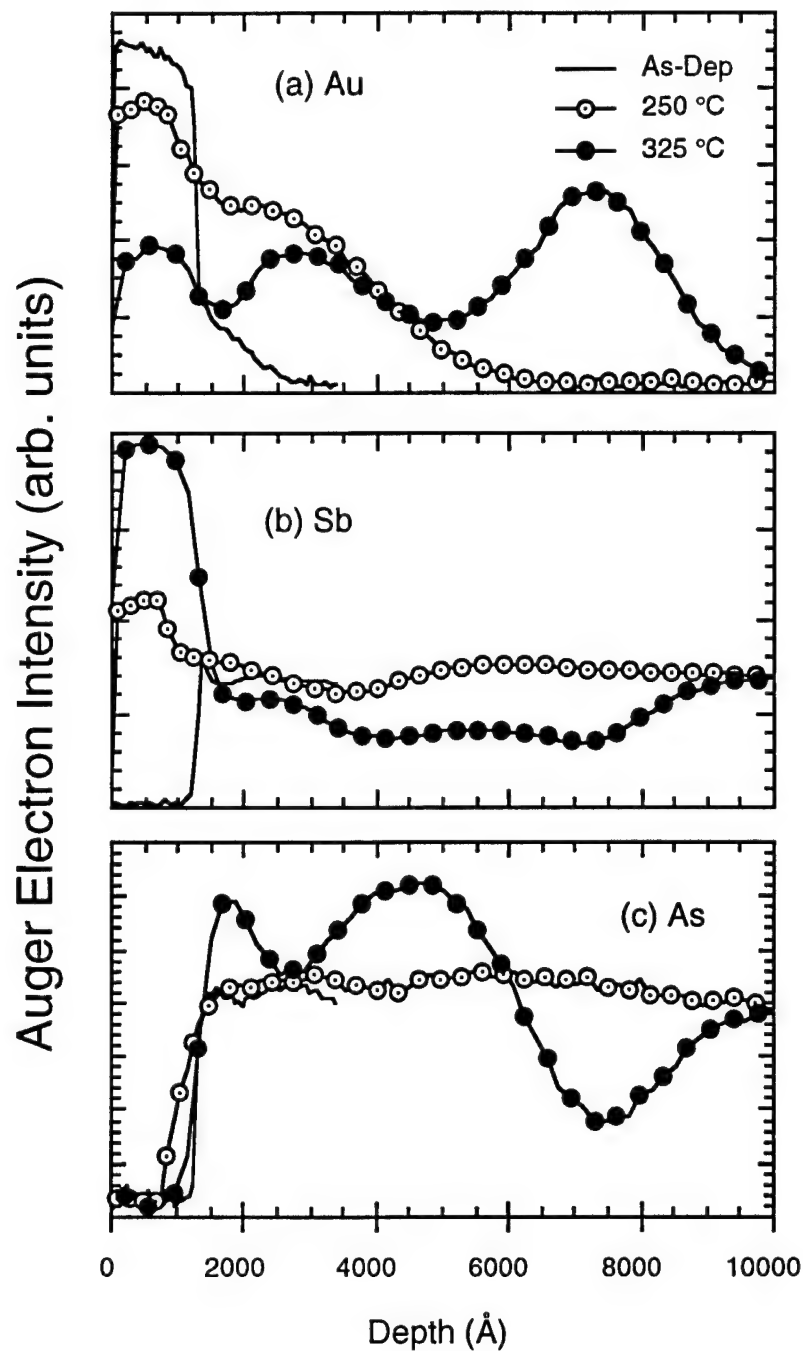


Figure 6.13. Auger electron spectroscopy depth profiles for Au/Zn/Au (50/200/1000 Å) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The spectra were measured following deposition, and following RTA at $T = 250^\circ\text{C}$ or 325°C for 30 seconds. The (a) Au, (b) Sb, and (c) As depth profiles are shown.

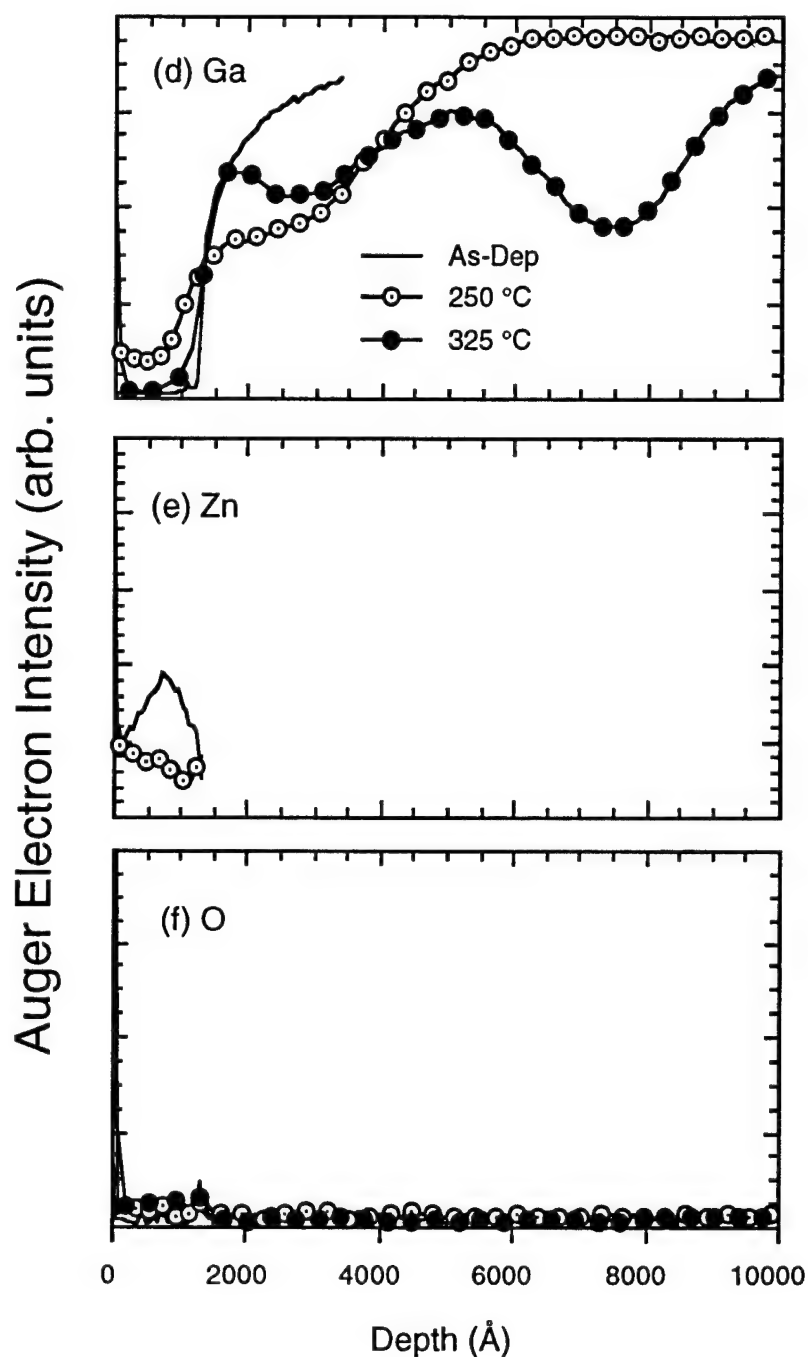


Figure 6.13 (cont.). Auger electron spectroscopy depth profiles for Au/Zn/Au (50/200/1000 Å) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. The spectra were measured following deposition, and following RTA at $T = 250\text{ }^{\circ}\text{C}$ or $325\text{ }^{\circ}\text{C}$ for 30 seconds. The (d) Ga, (e) Zn, and (f) O depth profiles are shown. Interference from the Ga Auger signal prevented detection of Zn in all spectra.

increased at the sample surface following RTA. The AES depth profiles permit some summary observations: (1) Au indiffuses deeply, (2) Sb outdiffuses and masses at the sample surface, and (3) regions where indiffused Au accumulates are deficient in Ga and As.

6.4.3 X-Ray Diffraction and XTEM Results. X-ray diffraction (XRD) was used to determine phase formation following Au/Zn/Au deposition and RTA. Glancing angle XRD measurements were obtained using a Rigaku D/max-1B diffractometer equipped with a thin film detachment and a monochromator. Copper-K α radiation ($\lambda = 1.5405 \text{ \AA}$) was used with a 40 kV acceleration potential and a 30 mA beam current. A fixed angle of $\theta = 5^\circ$ was maintained for the incoming beam. Reflected intensity was measured by an electronic counter which was stepped angularly in increments of 0.05° . Crystallographic planes were identified using standards from the International Center for Diffraction Data (ICDD) [32] and the JADE analysis program [33]. Cross-sectional transmission electron microscopy samples were prepared by mechanical thinning followed by ion milling as per Reference 34. XTEM and SAD were performed in a Hitachi H-600 scanning transmission electron microscope operated at 100 kV. The electron beam used to obtain selected area diffraction patterns has a beam diameter of approximately 1500 \AA . EDX was accomplished in a Phillips 400 electron microscope equipped with a field emission gun. The probe size used for EDX was approximately 1000 \AA in diameter.

Figure 6.14 contains XRD results for the Au/Zn/Au contact. Diffraction peaks are labeled according to the element or compound identified by the ICDD Powder Diffraction File. The intensity scale was expanded to allow observation of low intensity peaks normally suppressed when plotted on the same scale as the GaAs_{0.51}Sb_{0.49} peak. The as-deposited sample and the sample annealed at $T = 250^\circ \text{C}$ demonstrated only Au and GaAs_{0.51}Sb_{0.49} diffraction peaks. The five sets of Au diffraction peaks from low to high angle correspond to {111}, {200}, {220}, {311} and {222} fcc lattice planes. The Au

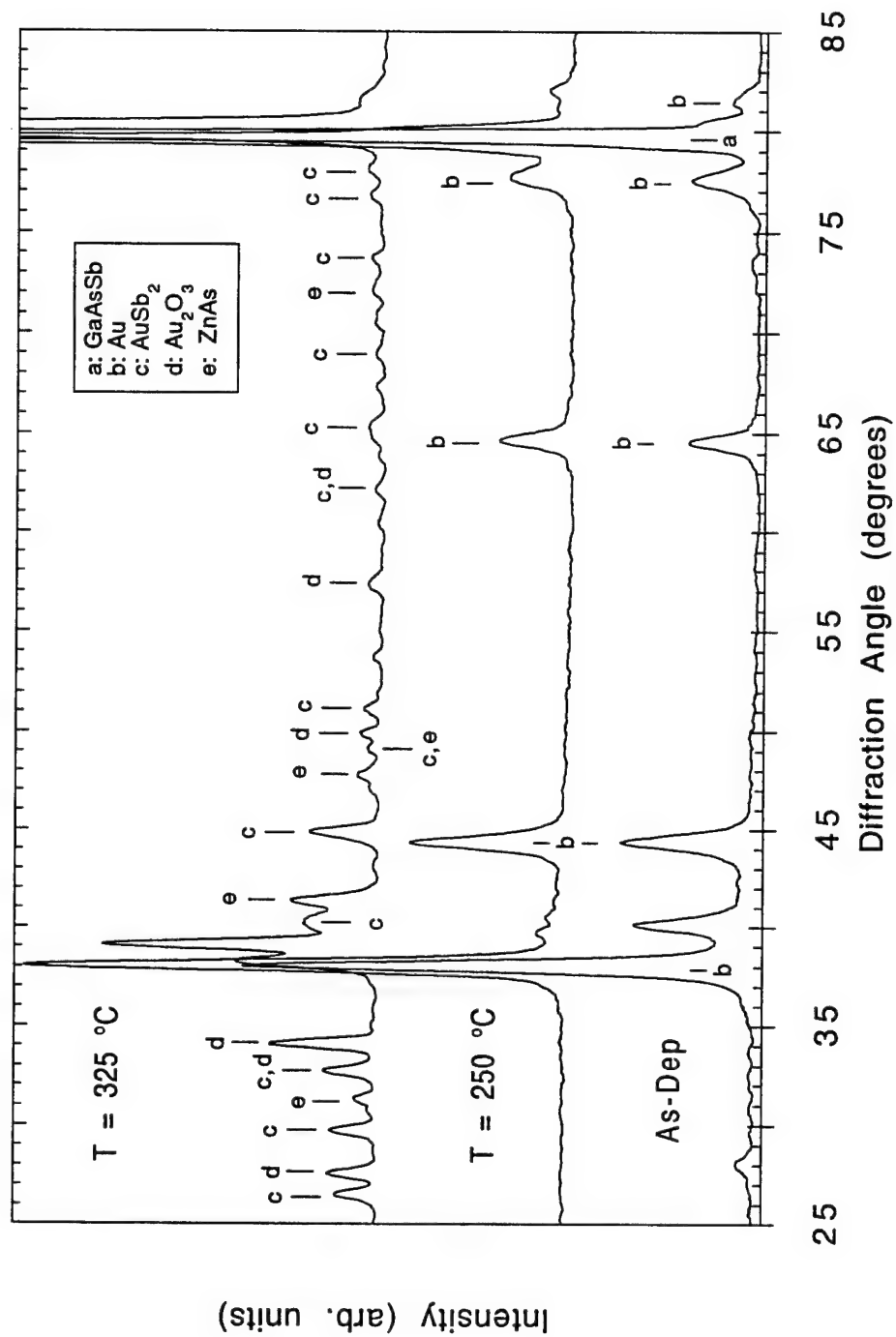


Figure 6.14 XRD spectra for Au/Zn/Au (50/200/1000 Å) on GaAs_{0.51}Sb_{0.49} measured following metal deposition and RTA at 250 °C or 325 °C. Labeled peaks correspond to the phases identified in the inset.

peaks correspond to a unit cell dimension of $a_0 = 4.045 \text{ \AA}$ which is 0.7% below the ICDD value [28]. No diffraction was detected from the Zn layer which indicates the Zn layer may be amorphous. Following RTA at $T = 325 \text{ }^\circ\text{C}$, the smallest Au diffraction peaks disappeared while only the {111} peak remained. Additionally, numerous diffraction peaks emerged and were identified with standards. The predominant phase was AuSb_2 with diffraction from simple cubic planes of $a_0 = 6.717 \text{ \AA}$ (0.9 % above nominal). Other diffraction peaks corresponded to Au_2O_3 and ZnAs . The XRD results indicate the predominant effect of RTA at $T = 325 \text{ }^\circ\text{C}$ is a reduction in Au and an increase in AuSb_2 .

XTEM, SAD and EDX characterization were performed following completion of the XRD measurements. A peculiar result emerged - no detectable difference was observed between as-deposited samples and samples annealed at $T = 250 \text{ }^\circ\text{C}$ for 30 seconds. Both contained a reacted layer beneath the surface metallization layer. The appearance of a reacted layer in the as-deposited sample seemed anomalous. However, three sets of nominally as-deposited samples were prepared and measured with same result. Therefore, numerous efforts were taken to assure the validity and repeatability of as-deposited samples.

Figures 6.15(a) through 6.15(c) provide XTEM and SAD results representing both the nominally as-deposited samples, and samples annealed at $T = 250 \text{ }^\circ\text{C}$. XTEM showed definitive microstructural layers: a top layer, a reacted layer containing dark protrusions and $\text{GaAs}_{0.51}\text{Sb}_{0.49}$, a $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layer, and InP substrate. The top layer was composed of two regions: a thinner region approximately 800 \AA thick, and a thicker region approximately 900 \AA to 1400 \AA thick. The thinner region is in the center of the micrograph while the thicker region is on the right side. The thinner region of the top layer was rich in Au and Zn as per EDX measurements while the thicker region was rich in Au, Sb and Zn. The reacted layer contained protrusions into the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ to depths 5100 \AA past the top layer. The protrusions are the dark regions in the figure. Figures 6.15(b) and 6.15(c)

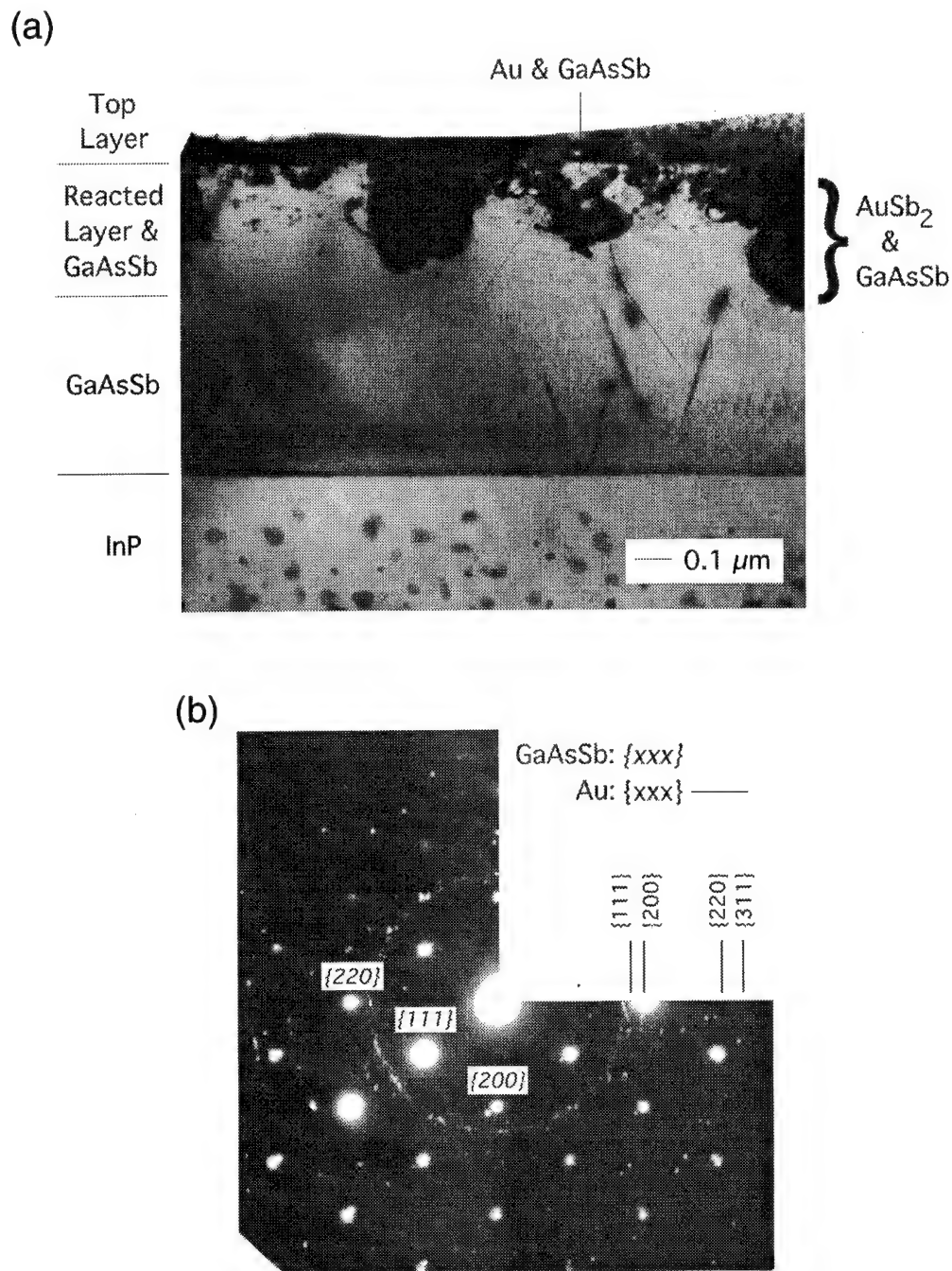


Figure 6.15 Transmission electron microscopy results for Au/Zn/Au (50/200/1000 Å) on Be-implanted GaAs_{0.51}Sb_{0.49}: (a) cross-sectional micrograph, and (b) selected area diffraction (SAD) pattern from a region containing Au and GaAs_{0.51}Sb_{0.49}. One quadrant of the SAD pattern is eliminated to identify Au diffraction rings. GaAs_{0.51}Sb_{0.49} crystallographic planes are identified in italic immediately above the corresponding diffraction spot. The cross-sectional micrograph and diffraction pattern were obtained on both nominally as-deposited, unannealed samples and samples subjected to RTA at T = 250 °C (30 sec).

(c)

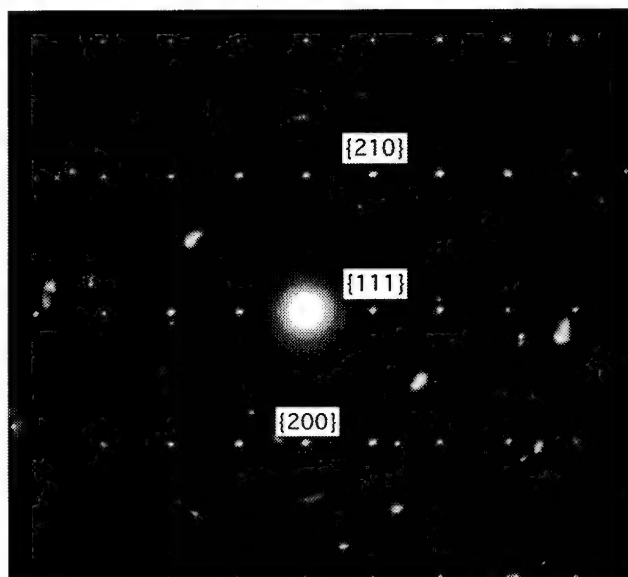


Figure 6.15 (cont.). Transmission electron microscopy results for Au/Zn/Au (50/200/1000 Å) on Be-implanted GaAs_{0.51}Sb_{0.49}: (c) selected area diffraction (SAD) pattern from a region containing AuSb₂. The AuSb₂ crystallographic planes are identified immediately above the corresponding diffraction spot. The SAD pattern was obtained on both nominally as-deposited, unannealed samples and samples subjected to RTA at T = 250 °C (30 sec).

are SAD patterns taken within the reacted layer. Figure 6.15(b) resulted from placing the electron beam in the center of the light colored region immediately beneath the top layer. This region is labeled "Au & GaAsSb" in Figure 6.15(a). The SAD picture demonstrated ring patterns from the {111}, {200}, {220}, and {311} family of polycrystalline Au planes. Also, numerous diffraction spots from single crystal GaAs_{0.51}Sb_{0.49} were measured. Diffraction spots from the {111}, {200} and {220} family of planes of GaAs_{0.51}Sb_{0.49} are labeled in *italic*. Figure 6.15(c) was obtained by placing the electron beam in the dark protrusion labeled "AuSb₂ & GaAsSb" shown at the right of Figure 6.15(a). The predominant diffraction spots were from AuSb₂ with $a_0 = 6.78 \text{ \AA}$ (1.8 % above nominal). The {111}, {200} and {210} family of planes for AuSb₂ are labeled while other AuSb₂ diffraction spots appear in horizontal rows in the figure. Beneath the reacted layer is a layer of GaAs_{0.51}Sb_{0.49} followed by the InP substrate. Some threading dislocations are evident in the GaAs_{0.51}Sb_{0.49} and may result from lattice strain during epitaxial growth or implant RTA. The dark centers in the InP are In clusters caused by ion milling during sample preparation and do not represent defects [35]. These results show RTA at $T = 250 \text{ }^\circ\text{C}$ causes Au indiffusion, Sb outdiffusion and formation of AuSb₂. Discussion of the similarity between the as-deposited and $T = 250 \text{ }^\circ\text{C}$ cases is deferred until Section 6.5.

Figure 6.16 provides the XTEM and SAD results for the Au/Zn/Au sample subjected to RTA at $T = 325 \text{ }^\circ\text{C}$. Much deeper diffusion was observed compared to the $T = 250 \text{ }^\circ\text{C}$ case. Three layers were identified by XTEM: a reacted layer containing GaAs_{0.51}Sb_{0.49}, a GaAs_{0.51}Sb_{0.49} layer, and the InP substrate. The reacted layer contained striated regions labeled "Region 1", and dark precipitates of varying shapes and sizes which are labeled "Region 2" in the figure. The precipitates were located at depths as deep as 8000 \AA below the sample surface. The precipitate regions were Au-rich as per EDX. Region 1 contained many dislocations. Region 1 was also Au deficient and rich in

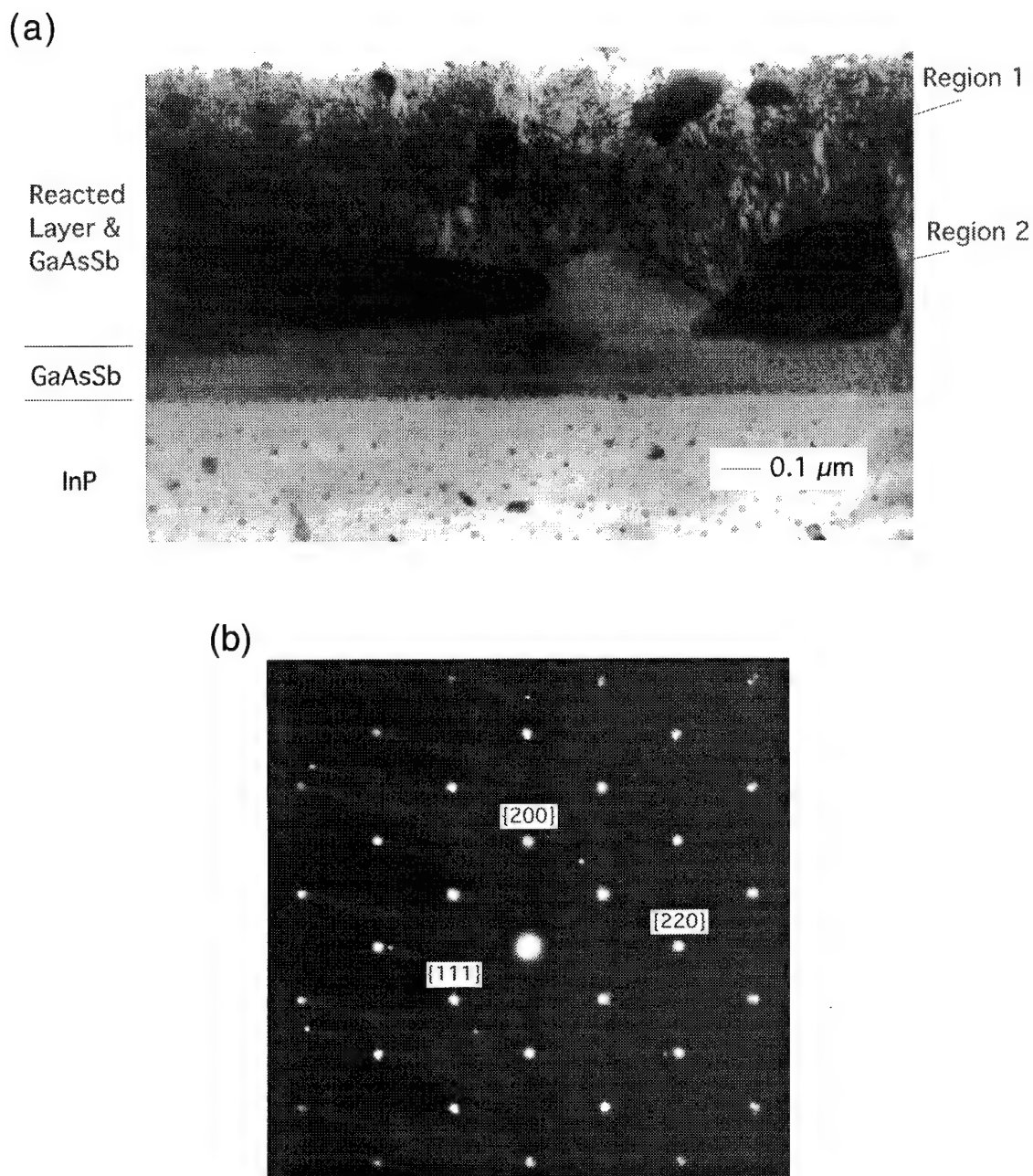


Figure 6.16 Transmission electron microscopy results for Au/Zn/Au (50/200/1000 Å) on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ following RTA at $T = 325^\circ\text{C}$ for 30 sec: (a) cross-sectional micrograph, and (b) selected area diffraction (SAD) pattern encompassing regions 1 and 2. $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ crystallographic planes are identified immediately above the corresponding diffraction spot.

Ga, As and Sb as per EDX. SAD patterns obtained in both Regions 1 and 2 were essentially the same. The SAD pattern shown in Figure 6.16(b) is therefore representative of both regions. The pattern showed bright diffraction spots from $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. Diffraction spots from the {111}, {200} and {220} family of planes are labeled in the figure. Other low intensity diffraction spots were also observed. These diffraction spots were too numerous and random in orientation to assign to crystallographic planes of particular phases. These results indicate that Au diffuses deeply into the sample following RTA at $T = 325\text{ }^{\circ}\text{C}$. The Au forms in precipitate regions and appears to produce dislocations in the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ epilayer.

6.5 Discussion of Experimental Results

The Au/Zn/Au contact is unsuitable for application to Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$. Considerable change in the electrical and microstructural properties occurs over a relatively low and narrow temperature range: $250\text{ }^{\circ}\text{C} \leq T \leq 325\text{ }^{\circ}\text{C}$. The experimental results also indicate degradatory metal-semiconductor reactions may take place at temperatures below $100\text{ }^{\circ}\text{C}$ as first explained in this section. Ohmic contact formation processes are next outlined for Au/Zn/Au on GaAs and GaSb. Finally, the observed degradation between Au/Zn/Au and $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ is described in terms of Au-Sb reactions.

XTEM measurements imply thermal instability may occur at temperatures as low as $T = 90\text{ }^{\circ}\text{C}$. XTEM demonstrated a similar reacted layer in as-deposited samples and samples annealed at $T = 250\text{ }^{\circ}\text{C}$. An additional thermal cycle occurs during XTEM sample processing. A hot plate bake at $T = 90\text{ }^{\circ}\text{C}$ for 6 hours is required to set a bonding epoxy prior to cross-sectional thinning of the sample. Consequently, the reacted layer observed in the nominally as-deposited sample appears to form at $T < 100\text{ }^{\circ}\text{C}$ during XTEM sample preparation.

Heating of the sample above 100 °C with concurrent formation of the reacted layer during metal evaporation is doubtful. First, the behavior of photoresist would expose sample heating above $T \geq 100$ °C during deposition. The 1400-17 photoresist is used to form metallization patterns. The deposition time for the 3000 Å thick Au top layer in TLM samples is approximately 20 minutes. Exposure to $T > 100$ °C for a period of 20 minutes or more would hardbake the 1400-17 photoresist. No difficulty was experienced in removing the 1400-17 photoresist using acetone following Au/Zn/Au evaporation. Hence hardbaking did not occur. Second, the adhesion of wax mounted samples indicates a temperature less than 100 °C during evaporation. Small samples are frequently wax mounted to 2"-dia. support wafers prior to deposition. The mounting wax liquefies at $T = 100$ °C. Consequently, temperatures of $T \geq 100$ °C would melt the wax and cause the samples to fall from the 2" mounting wafer during deposition. Third, AES profiles were distinctly different between the as-deposited and $T = 250$ °C cases and did not demonstrate a severe reaction between Au/Zn/Au and GaAs_{0.51}Sb_{0.49} until $T = 250$ °C. The as-deposited AES sample did not undergo heating to $T = 90$ °C as did the nominally as-deposited XTEM sample. Therefore, the reactive layer most likely forms at $T = 90$ °C during XTEM sample preparation.

Studies of Au/Zn/Au on GaAs have demonstrated some reproducible effects which assist in the identification of ohmic contact formation processes [2,4-6]. Minimum contact resistance on GaAs was realized at temperatures in the range $320 \leq T \leq 450$ °C [2,4,6,7]. The process is a balance between initial Au-Zn interactions at low temperature, and metal-semiconductor reactions at higher temperatures. The Zn layer tends to spread into the Au layer above the GaAs either during deposition or following temperatures as low as $T = 100$ °C during XTEM sample preparation [2,6]. This low temperature Zn diffusion causes formation of Au-Zn compounds: AuZn [2,6], Au₃Zn [5] or α -AuZn [6]. Ohmic contact formation occurs when the sample is further heated to $T \geq 300$ °C. Heating the sample

causes: (1) transformation of the original Au-Zn phase to a different Au-Zn phase in some cases (i.e. $\text{AuZn} + \alpha\text{-AuZn} \rightarrow \alpha_3\text{-AuZn}$ [6]), (2) penetration of GaAs surface oxides [2], (3) formation of Au-Ga compounds (i.e. $\alpha\text{-AuGa}$ [2]) , (4) p-type interfacial doping through Zn_{Ga} site formation [2,5,6], and (5) GaAs surface degradation in the event of excess As outdiffusion [4]. Ohmic contact is formed by penetration of the surface oxide and doping of Ga sites with Zn. Contact stability depends upon the ability of the Au-Zn compound to prevent As outdiffusion and getter Ga only within a few monolayers [4,6].

Reports examining the microstructural evolution of the Au/Zn/Au ohmic contact to p-GaSb [8,10] are less numerous than GaAs.* However, reports containing only electrical results are available [9,36]. Minimum contact resistance was obtained for GaSb at temperatures in the range $250 \leq T \leq 300$ °C [8,10,36]. Microstructural characterization results demonstrated indiffusion of Au, and outdiffusion of Zn, Ga and Sb towards the contact surface following heat treatment at $T = 300$ °C [8,10]. Formed in this reaction are Au-Ga and Au-Zn compounds, and AuSb_2 [10]. Studies of Au contacts to GaSb showed minimum contact resistance at $T = 200$ °C [37] or $T = 250$ °C [36] which rose rapidly with an increase in temperature. These results demonstrate: (1) a lower reaction temperature than that of Au/Zn/Au on GaAs (with a further reduction in reaction temperature when Au is applied directly to GaSb), (2) formation of Au-Sb compounds (unlike GaAs where Au-As compounds do not occur), and (3) a lack of Au-Zn compound formation at the metal-semiconductor interface. Consequently, the introduction of Sb on the Group III site produces tangibly different reactions for the Au/Zn/Au contact on GaSb compared to GaAs. These reactions for GaSb correlate with those of Au/Zn/Au on Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ - little reliance on Zn to form Au-Zn diffusion barriers and Zn-doped Ga sites, and an intense reaction with Au.

* The listed reports are also less in depth, containing no TEM results.

Observations from this present study indicate a fundamental degradation reaction occurs between Au and Sb and includes: (1) formation of AuSb_2 as per XTEM following sample preparation at 90 °C and RTA at $T = 250$ °C, and at $T = 325$ °C as per XRD, (2) a laterally diffusing surface layer as per SEM and TLM, and (3) deep Au indiffusion and Sb outdiffusion at $T = 250$ °C as per AES and XTEM. The potential for Au-Sb interactions in the temperature range $90\text{ °C} \leq T \leq 325\text{ °C}$ with subsequent formation of AuSb_2 is quite probable. The SIMS results of Figure 5.16 demonstrated a loss of surface Ga and As following Be implantation and RTA. Also, AES results of Figure 6.13 demonstrated a slight Au indiffusion and Sb peaking at the metal-semiconductor interface on the as-deposited sample. Thus a condition exists for Au-Sb reactions following implantation and metal deposition - Au penetration of a Sb-rich region. Experiments with deposited Au and Sb provide some insight upon the conditions required for AuSb_2 formation. The crystallization temperature of AuSb_2 depends upon the total layer thickness of the Au + Sb film when Au and Sb are codeposited [38]. AuSb_2 crystallizes at $T = 83$ °C for layers less than 60 Å thick. The crystallization temperature decreases as the layer thickness is increased. Crystallization causes a sharp drop in electrical resistance as Sb transitions from an amorphous to crystalline state [38,39]. A codeposited-type region less than 60 Å thick may exist in cases where Au has penetrated the Sb-rich $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. This region would conceivably crystallize during XTEM sample preparation at $T = 90$ °C. The sharp drop in contact resistance may also correspond with the crystallization of the AuSb_2 . The composition of the laterally diffusing surface layer is unknown as of this writing. The massive outdiffusion of Sb towards the contact surface and the formation of large protruding regions of AuSb_2 indicate either of these phases is the culprit. Indiffusing Au forms AuSb_2 protrusions at $90\text{ °C} \leq T \leq 250\text{ °C}$ which extend approximately 5000 Å into the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ layer as per XTEM micrographs. Formation of the AuSb_2 may break

Ga and As bonds, facilitating Ga and As diffusion into regions deficient in Au. Thus regions of modulating Au, Ga and As concentration may occur as seen in the AES results .

The addition of Zn in the metal system appears to have little effect on ohmic contact formation. No evidence of Zn was detected in the as-deposited XRD spectrum, indicating the layer may initially be amorphous. RTA at $T = 325\text{ }^{\circ}\text{C}$ produced the ZnAs compound. However, similar to the Au/Zn/Au-GaSb case, no Au-Zn compounds were formed in contrast to results for Au/Zn/Au on GaAs.

6.6 Chapter VI Summary

The Au/Zn/Au contact forms a low resistance ohmic contact to Be implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ with as-deposited contact resistances of $\rho_c < 2 \times 10^{-7}\text{ }\Omega\text{-cm}^2$. However, the Au/Zn/Au contact is thermally unstable. Microstructural characterization demonstrates instability is induced by the formation of AuSb_2 at temperatures as low as $T = 90\text{ }^{\circ}\text{C}$. RTA of the contact at $T = 325\text{ }^{\circ}\text{C}$ causes Au indiffusion to depths of $8000\text{ }\text{\AA}$ into the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ and outdiffusion of Sb to the sample surface. These results dictate that Au should not come into contact directly with the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. The thermal stability limitations imposed by the Au/Zn/Au contact are overcome by the Ti/Pt/Au nonalloyed ohmic contact as demonstrated in the following chapter.

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VII. Ti/Pt/Au Non-Alloyed Ohmic Contact to GaAsSb and the InAlAs/GaAsSb HIGFET

7.1 Introduction

Chapter VI demonstrated Au/Zn/Au as an unsuitable metallization for ohmic contact to Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$. Therefore, in order to prove the viability of the InAlAs/GaAsSb HIGFET, and warrant further research on this technology, another candidate metallization was selected and applied. This chapter demonstrates Ti/Pt/Au as a nonalloyed ohmic contact which provides a thermally stable, low resistance, electrical interface to Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$. Application of Be implantation and the Ti/Pt/Au ohmic contact improves the electrical performance and thermal stability of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET compared with previous designs using diffused Au/Zn/Au source/drain contacts.

The experimental approach and organization of this chapter essentially mirrors Chapter VI. Consequently, explanations of experimental methods common to both chapters are contained only in Chapter VI.

7.2 Ohmic Contact Preparation

Epitaxial growth, sample preparation and electrical testing were performed in the same manner as the Au/Zn/Au metallizations described in Section 6.2. All $\text{GaAs}_{1-x}\text{Sb}_x$ samples studied in this chapter were implanted with Be under the following conditions: $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$, $E = 50 \text{ keV}$, $\theta = 7^\circ$. The implanted samples were annealed at $T = 600^\circ\text{C}$ for 10 seconds. The Ti, Pt and Au layers were sequentially deposited by electron beam evaporation in a Temescal FC1800 system at pressures below 1×10^{-6} torr.

Layer thicknesses of 200/600/3000 Å were used to form Ti/Pt/Au contacts to TLM patterns and HIGFET devices. The selected layer thicknesses were based upon previous

results showing high thermal stability of Ti/Pt/Au contacts on $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ [1] and GaAs [2] through the use of a Pt layer of 500 Å or greater thickness. The 200 Å Ti layer permits adhesion of subsequent metals to the $\text{GaAs}_{1-x}\text{Sb}_x$. A 3000 Å top layer of Au was chosen as a thickness suitable for wire bonding. The anneal temperature was targeted to cover the range $250 \leq T \leq 450$ °C with a constant anneal time of 30 seconds. This temperature range was selected based upon anneal temperatures used for Ti/Pt contacts on p-type GaAs [3,4], $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [5], InAs [6] and other III-V semiconductors [7,8].

7.3 Electrical Characterization Results

7.3.1 TLM Results. The initial TLM test determined the behavior of the Ti/Pt/Au contact with respect to RTA temperature. The average values of contact resistance (R_c), sheet resistance (R_{sh2}) and specific contact resistance (ρ_c) are depicted in Figure 7.1. A low average contact resistance was measured following deposition: $R_c = 0.086$ Ω-mm ($\rho_c = 2.76 \times 10^{-7}$ Ω-cm²). The average contact resistance dropped following RTA at $T = 225$ °C for 30 seconds. A minimum contact resistance of $R_c = 0.021$ Ω-mm ($\rho_c = 1.82 \times 10^{-7}$ Ω-cm²) was obtained after annealing at $T = 250$ °C. Contact resistance was maintained below 0.1 Ω-mm for RTA temperatures of $T \leq 450$ °C. RTA at $T = 475$ °C caused a nonuniform increase in raw resistance values measured between the Ti/Pt/Au metallization spacings with no observed electrical shorting. Poor correlation resulted in the TLM data and accurate measurement of the contact resistance was thus prevented. Average sheet resistance remained essentially constant over the wide anneal temperature range: $278 \text{ Ω/sq} \leq R_{sh2} \leq 288 \text{ Ω/sq}$. The steady sheet resistance indicates no corruption of the $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ in the region between the Ti/Pt/Au contacts. These results demonstrated the Ti/Pt/Au has a low as-deposited contact resistance value. Sintering these contacts at $T = 250$ °C minimizes the contact resistance. The contact resistance remains low and below the as-deposited value over a wide temperature range $225 \text{ °C} \leq T \leq 450 \text{ °C}$. Sheet

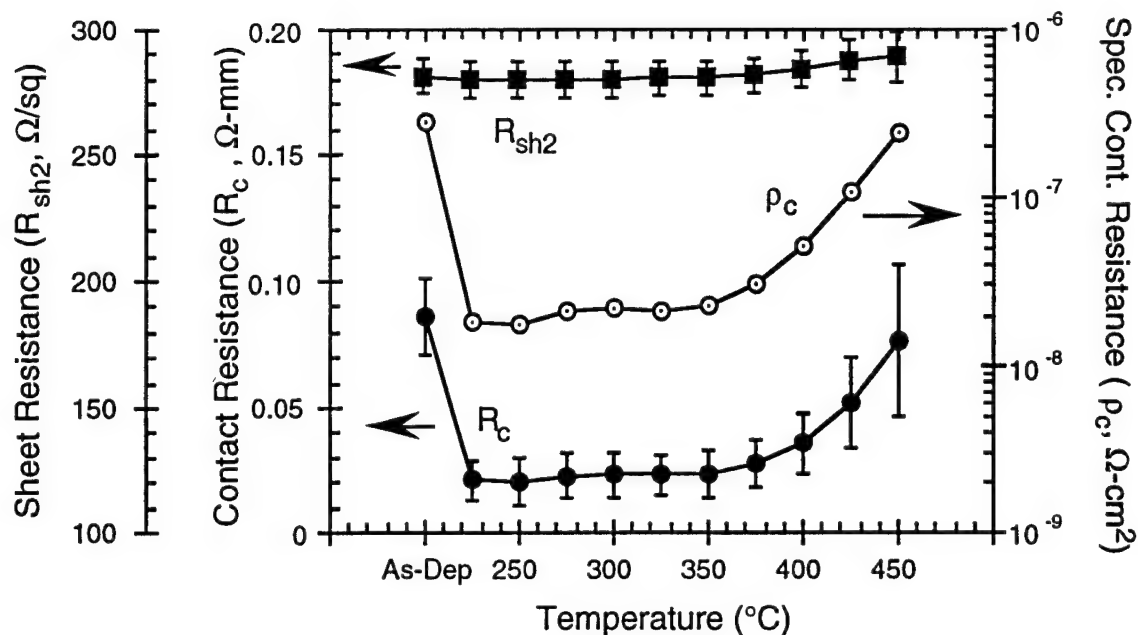


Figure 7.1. Contact resistance (R_c , $\Omega\text{-mm}$), sheet resistance (R_{sh2} , Ω/sq) and specific contact resistance (ρ_c , $\Omega\text{-cm}^2$) for Ti/Pt/Au (200/600/3000 \AA) on Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ as a function of RTA temperature. Isochronal annealing (30 seconds) was sequentially performed on the sample. Error bars indicate one standard deviation. Measurements were made at room temperature.

resistance measurements indicate degradation of the $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ does not occur due to lateral migration of metallization components.

TLM measurements were next taken to determine the sensitivity of the Ti/Pt/Au contact with respect to RTA time. A $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ sample with Ti/Pt/Au was sequentially subjected to anneal times between 5 seconds and 5 minutes duration at $T = 250^{\circ}\text{C}$. The 250°C temperature was chosen since it produced the lowest R_c value during isochronal RTA. Figure 7.2 illustrates the average values of contact resistance and sheet resistance measured after RTA.* A five second RTA decreased the average contact resistance from an as-deposited value of $R_c = 0.074 \Omega\text{-mm}$ ($\rho_c = 1.54 \times 10^{-7} \Omega\text{-cm}^2$) to R_c

* For clarity, a 90 second anneal time means the sample received a full 90 second anneal at $T = 250^{\circ}\text{C}$. Anneal times shown in Figure 7.2 are not the sum of previous anneal times.

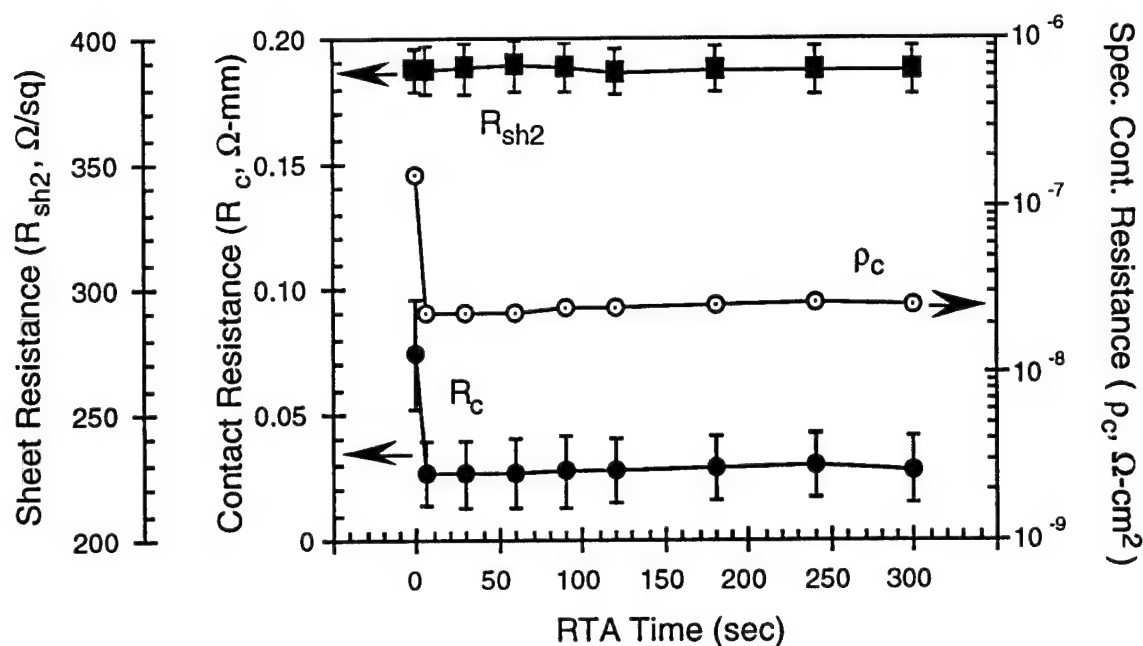


Figure 7.2. Contact resistance (R_c , $\Omega\text{-mm}$), sheet resistance (R_{sh2} , Ω/sq) and specific contact resistance (ρ_c , $\Omega\text{-cm}^2$) for Ti/Pt/Au (200/600/3000 Å) on Be-implanted $\text{GaAs}_{0.53}\text{Sb}_{0.47}$ as a function of RTA time. The sample was sequentially annealed at $T = 250^\circ\text{C}$ for each time indicated. Measurements were made at room temperature.

$= 0.027 \Omega\text{-mm}$ ($\rho_c = 2.27 \times 10^{-8} \Omega\text{-cm}^2$). The average contact resistance remained essentially constant after RTA at $T = 250^\circ\text{C}$ for times up to five minutes. The sheet resistance was basically unchanged following deposition and RTA over the time range shown. This isothermal annealing study shows the Ti/Pt/Au contact again has low, as-deposited contact resistance. The contact resistance is reduced considerably by sintering of the contact at $T = 250^\circ\text{C}$ in a thermal cycle as short as five seconds in duration.

Long term thermal storage was next performed on the Ti/Pt/Au ohmic contact. The basis of the long term thermal storage is to elevate the ambient temperature above that which the contact would normally encounter. Degradation mechanisms, otherwise dormant at room temperature, are accelerated and become apparent in a shorter time span. The contact resistance and sheet resistance results are shown in Figure 7.3. TLM

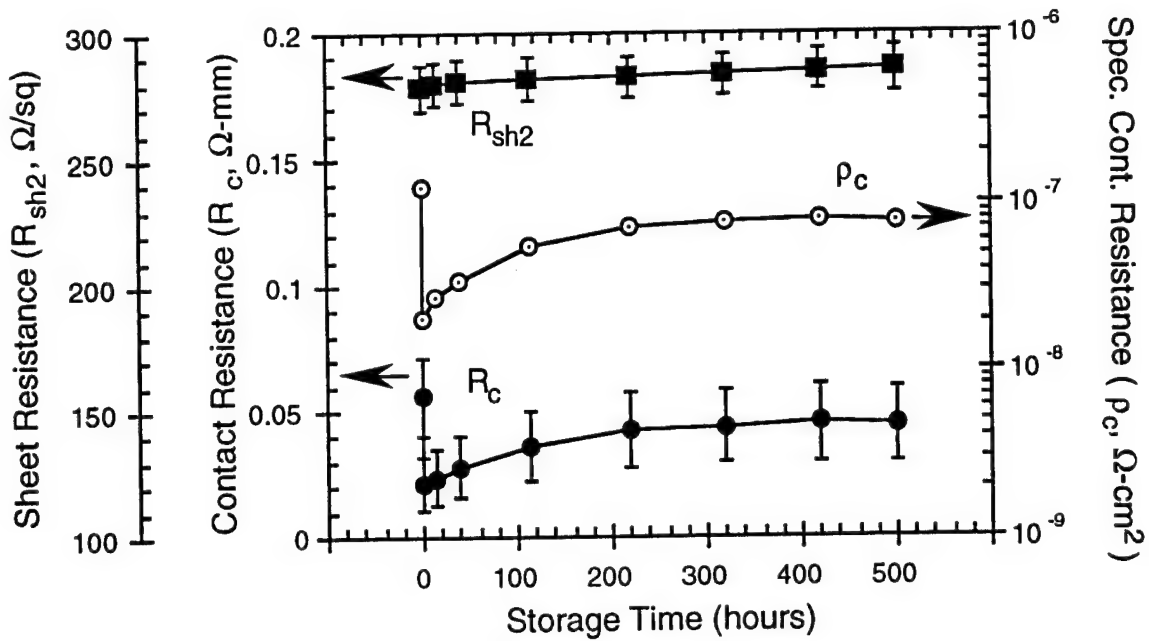


Figure 7.3. Contact resistance (R_c , $\Omega\text{-mm}$), sheet resistance (R_{sh2} , Ω/sq) and specific contact resistance (ρ_c , $\Omega\text{-cm}^2$) for Ti/Pt/Au (200/600/3000 Å) on Be-implanted GaAs_{0.46}Sb_{0.54} as a function of thermal storage time. Measurements were made at room temperature following thermal storage at $T = 250^\circ\text{C}$. Storage times are cumulative.

measurements were taken at room temperature following storage at $T = 250^\circ\text{C}$ for the cumulative times shown. The total storage time for the Ti/Pt/Au sample was 500 hours. An initial reduction in R_c from $0.056 \Omega\text{-mm}$ ($\rho_c = 1.23 \times 10^{-7} \Omega\text{-cm}^2$) to $0.022 \Omega\text{-mm}$ ($\rho_c = 2.03 \times 10^{-8} \Omega\text{-cm}^2$) was encountered after one hour of storage. Thereafter, R_c increased with storage time. The contact resistance had the sharpest increase between 1 and 13 hours. However, the increase in R_c lessened after each successive interval. Contact resistance was essentially constant after storage at 500 hours with $R_c = 0.045 \Omega\text{-mm}$ ($\rho_c = 7.64 \times 10^{-8} \Omega\text{-cm}^2$). The contact resistance after 500 hours is still well below $R_c = 0.1 \Omega\text{-mm}$. Sheet resistance increased only slightly during the entire thermal storage procedure, from $R_{sh2} = 279 \Omega/sq$ to $285 \Omega/sq$, indicating the channel region was essentially unaffected

by the experiment. These results show the Ti/Pt/Au contact maintains a very low contact resistance and is thermally stable for up to 500 hours.

7.3.2 Thermal Measurements on the Ti/Pt/Au Ohmic Contact. The specific contact resistance of the Ti/Pt/Au ohmic contact was measured under a varying ambient temperature. The measurement method was the same used in Section 6.3.2. A plot of $\rho_c \cdot T$ versus $1/T$ is shown in Figure 7.4. Three cases were studied for the Ti/Pt/Au contact: as-deposited, and following RTA at $T = 250^\circ\text{C}$ or 375°C for 30 seconds. These two RTA temperatures were selected from the results shown in Figure 7.1. The temperatures represent the case where minimum contact resistance is encountered with respect to RTA temperature, and the case where the contact begins to deteriorate electrically without complete degradation. The same TLM sites were measured following each RTA cycle. A linear, least squares fit to the as-deposited data points was obtained using Equation 6.3. Hence, thermionic emission dominates throughout the as-deposited, contact area. The least squares fit produced $\phi_{BP} = 0.022\text{ eV}$ and $A^{**} = 1.16\text{ A/(K}^2\text{cm}^2\text{)}$. Thus a very small barrier height was detected in the as-deposited Ti/Pt/Au contact. The barrier height is almost equal to that of the as-deposited Au/Zn/Au contact where $\phi_{BP} = 0.021\text{ eV}$. The measured values of $\rho_c \cdot T$ no longer plotted in an Arrhenius fashion following RTA at $T = 250^\circ\text{C}$ or 375°C . Both cases deviated slightly from complete linearity, indicating a non-thermionic component is present in the total specific contact resistance.

Specific contact resistance is plotted directly against ambient measurement temperature in Figure 7.5. The figure shows experimentally measured ρ_c values subsequently modeled by a least squares fit to Equation 6.4. The electrical behavior of the contact was consistent with that of Figure 7.1. Namely, the contact resistance is minimum following RTA at $T = 250^\circ\text{C}$ and increases after RTA at 375°C .

A summary of the least squares fitting results is provided in Table 7.1. The thermionic nature of the as-deposited Ti/Pt/Au contact is reiterated in the first line of the

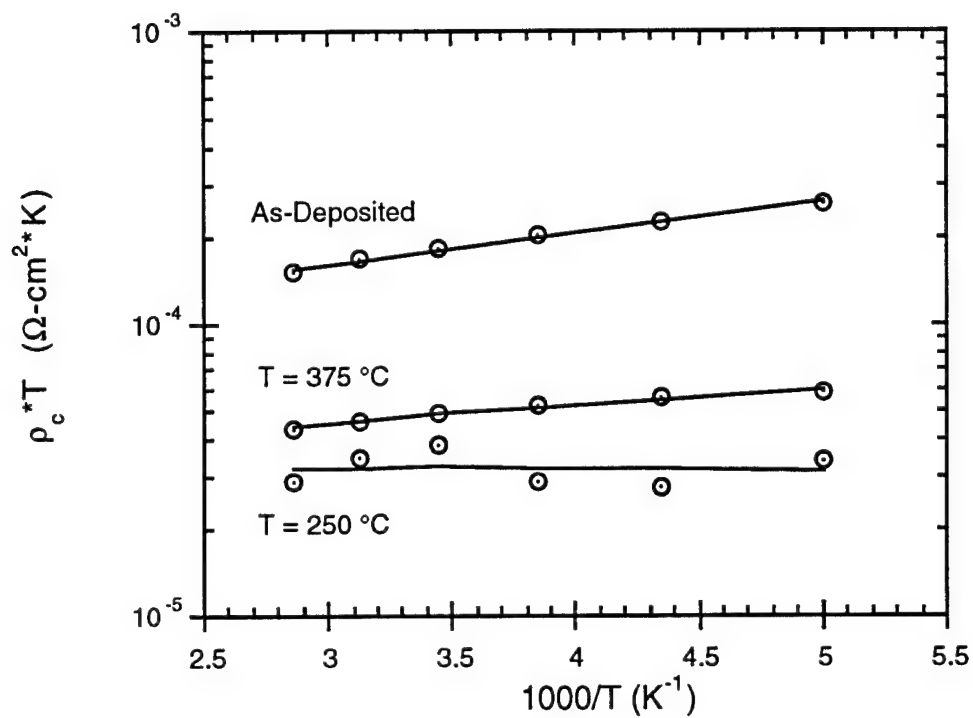


Figure 7.4. The product of specific contact resistance and temperature versus the reciprocal of ambient measurement temperature for Ti/Pt/Au (200/600/3000 Å) on Be-implanted GaAs_{0.46}Sb_{0.54}. The data points represent average, measured values of ρ_c . The three data sets are for the as-deposited case and following RTA at T = 250 °C or 375 °C for 30 seconds.

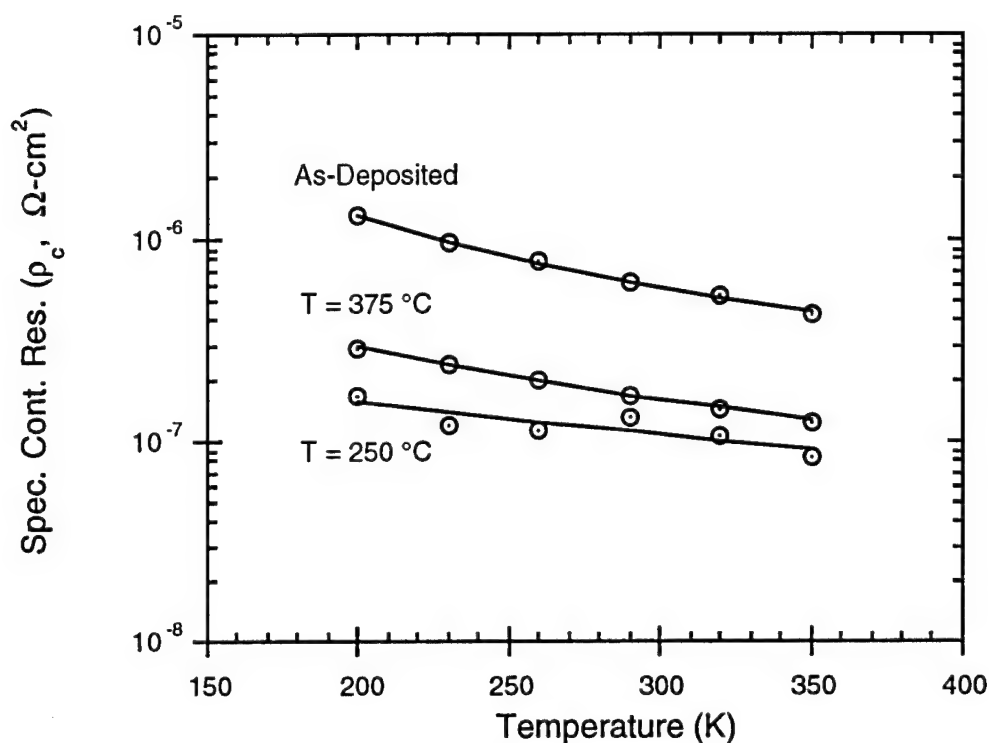


Figure 7.5. Specific contact resistance versus ambient measurement temperature for Ti/Pt/Au (200/600/3000 Å) on Be-implanted GaAs_{0.46}Sb_{0.54}. The data points represent average, measured values of ρ_c . The solid lines represent least squares fits to the experimental data points using Equation 6.4. The three data sets are for the as-deposited case and following RTA at T = 250 °C or 375 °C for 30 seconds.

Table 7.1. Summary of Metal-Semiconductor Transport Parameters: Ti/Pt/Au Ohmic Contact on Beryllium-Implanted GaAsSb

Deposition or RTA Condition	ϕ_{BP} (eV)	A^{**} [$A/(K^2cm^2)$]	A_f (no units)	ρ_{cf} ($10^{-8} \Omega\text{-cm}^2$)
As-Deposited	0.022	1.16	0.0	N/A
250 °C, 30 sec	0.022	4.05	0.138	3.36
375 °C, 30 sec	0.022	3.58	0.059	4.93

table. The table shows the barrier height of the thermionic region of the contact remained constant at $\phi_{BP} = 0.022$ eV following each of the two RTA cycles. The effective Richardson constant increased following RTA at $T = 250$ °C and decreased slightly after RTA at $T = 375$ °C. The area of the contact dedicated to field emission increased to $A_f = 13.8$ % following the 250 °C RTA and decreased to 5.9 % after RTA at $T = 375$ °C. The specific contact resistance of the field emission region was $\rho_{cf} = 3.36 \times 10^{-8} \Omega\text{-cm}^2$ at $T = 250$ °C and increased to $4.93 \times 10^{-8} \Omega\text{-cm}^2$ after RTA at $T = 375$ °C. These results show the field emission region maximized in area (A_f) and minimized in specific contact resistance (ρ_{cf}) after RTA at 250 °C. Correspondingly, ρ_c was minimized through RTA at $T = 250$ °C through the introduction of a lower resistance, parallel current path. Increased ρ_c at an RTA temperature of 375 °C is caused by: (1) decreasing field emission area with a higher ρ_{cf} , and (2) the decrease in A^{**} . The reduction in A^{**} raises ρ_{cth} over the entire ambient measurement temperature range. These thermal probe results demonstrate the Ti/Pt/Au-GaAs_{0.46}Sb_{0.54} interface is electrically well behaved to RTA temperatures of $T = 375$ °C. The barrier height is consistent with only slight variations in A^{**} . Consequently, large changes in microstructure are not anticipated for RTA temperatures below 375 °C based upon these electrical measurements.

7.4 Microstructural Characterization of the Ti/Pt/Au Ohmic Contact

This section presents microstructural characterization results obtained on Ti/Pt/Au (200/600/1000 Å) films on GaAs_{0.49}Sb_{0.54} after RTA. The samples used in each characterization method originated from the same, 2" diameter, (100) InP:Fe wafer. The GaAs_{0.46}Sb_{0.54} epilayer thickness was nominally 0.5 µm. The Be ion implantation and anneal procedure were performed as previously described in Section 5.3 (implant: $E = 50$ keV, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$; RTA: $T = 600$ °C, $t = 10$ seconds). The Au surface layer was reduced to 1000 Å thick to facilitate microscopies which require penetration of this layer

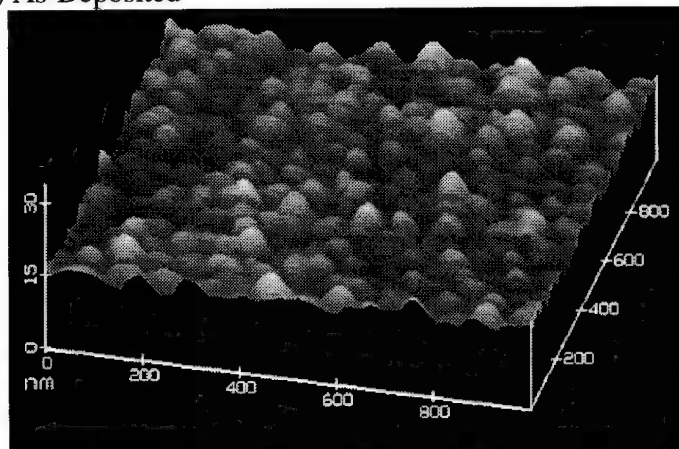
such as XRD and AES. The Ti/Pt/Au samples were evaluated following metal deposition and after RTA at $T = 250^{\circ}$ or 475°C for 30 seconds. These RTA temperatures were selected based upon the results of Figure 7.1. These three temperatures represent the initial metal-semiconductor construction, the RTA temperature which minimizes R_c , and the RTA temperature which causes thorough electrical and observational degradation. Sample preparation and measurement procedures are the same as described in Section 6.4 unless otherwise noted.

7.4.1 Atomic Force Microscopy Results. Atomic force micrographs of the Ti/Pt/Au surface are shown in Figures 7.6(a) through 7.6(c). Table 7.2 presents statistical measurements of the root-mean-square (rms) roughness, peak-to-valley roughness and grain diameter size corresponding to Figure 2.6.

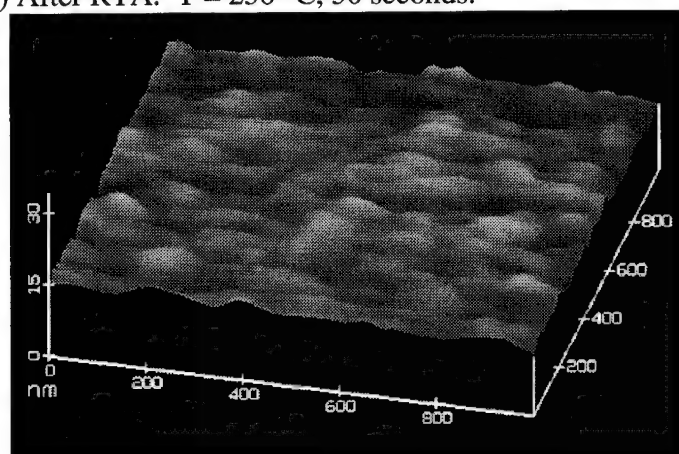
The AFM results showed a smoother surface with larger Au grains following RTA at $T = 250^{\circ}\text{C}$. The rms surface roughness decreased from $\pm 13 \text{ \AA}$ to $\pm 10 \text{ \AA}$ following the $T = 250^{\circ}\text{C}$ thermal cycle. Also, grain diameter size range at the Au surface increased approximately four times over the as-deposited value. Simultaneous reduction in roughness and extension of the grain size means the surface is more smooth and uniform. Thus both contact resistance and surface morphology are improved by the RTA at $T = 250^{\circ}\text{C}$. A smooth and uniform surface permits subsequent deposition of higher levels of interconnect metallization such as Ti/Au or Au.

A considerable increase in the surface roughness was observed and statistically measured following RTA at $T = 475^{\circ}\text{C}$. The rms roughness increased to $\pm 646 \text{ \AA}$ with an increase in grain size diameter range to $0.190 - 1.81 \mu\text{m}$. Figure 7.6(c) demonstrates these results pictorially. The peak-to-valley roughness of nearly 6000 \AA negates achievement of planarized interconnect metallizations. Increases in both grain size and overall surface nonuniformity were measured compared with the previous two micrographs.

(a) As-Deposited



(b) After RTA: $T = 250\text{ }^{\circ}\text{C}$, 30 seconds.



(c) After RTA: $T = 475\text{ }^{\circ}\text{C}$, 30 seconds.

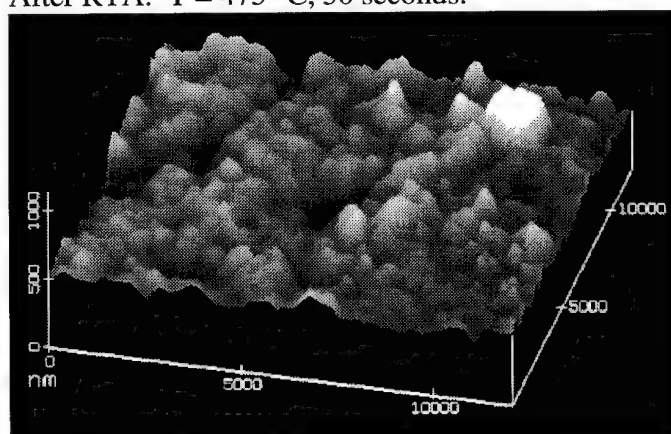


Figure 7.6. Atomic force micrographs of Ti/Pt/Au (200/600/1000 Å) surface: (a) as-deposited, and following RTA at (b) 250 °C or (c) 475 °C for 30 seconds. All scales are in nanometers. [Note scale change on micrograph (c).]

Table 7.2. Summary of Surface Roughness by Atomic Force Microscopy:
Ti/Pt/Au on Beryllium-Implanted GaAsSb

Deposition or RTA Condition	RMS Roughness (Å)	Pk-Val Roughness (Å)	Grain Dia. (μm)
As-Deposited	±13	101	0.023 - 0.061
250 °C, 30 sec	±10	88	0.069 - 0.290
475 °C, 30 sec	±646	5892	0.190 - 1.81

Hence, both the contact resistance and surface of the Ti/Pt/Au contact are degraded by thermal processing at $T = 475\text{ }^{\circ}\text{C}$, rendering the contact unsuitable for further use.

7.4.2 Auger Electron Spectroscopy Results. Auger electron spectroscopy was performed on the Ti/Pt/Au samples in order to obtain elemental depth profiles. The measurement process was the same as in Section 6.4.2, except Pt-MNN (1967 eV) and Ti-LMM (418 eV) Auger transitions were monitored. Figures 7.7(a) through 7.7(g) provide the AES spectra for the elements Au, Pt, Ti, Ga, As, Sb and O.

Little or no change occurred in the AES spectra following RTA at $T = 250\text{ }^{\circ}\text{C}$. Each metal layer was separately identifiable in the Au, Pt and Ti profiles. The Ga and As semiconductor elements demonstrated well defined, abrupt interfaces below the Ti. A small ledge in the Sb profile occurred just below the Ti layer. This small ledge is evidence of an excess of Sb at the metal semiconductor interface following implantation. The Ti profile indicated a slight indiffusion at $T = 250\text{ }^{\circ}\text{C}$ as represented by the decreased peak intensity and shift of the profile edge towards the $\text{GaAs}_{0.46}\text{Sb}_{0.54}$. A very small O signal was detected between the Ti and the $\text{GaAs}_{0.46}\text{Sb}_{0.54}$. (The as-deposited O peak intensity was approximately 5 % of the peak Ti signal intensity). The O concentration at the interface decreased following RTA at $T = 250\text{ }^{\circ}\text{C}$. The changes in the Ti and O spectra

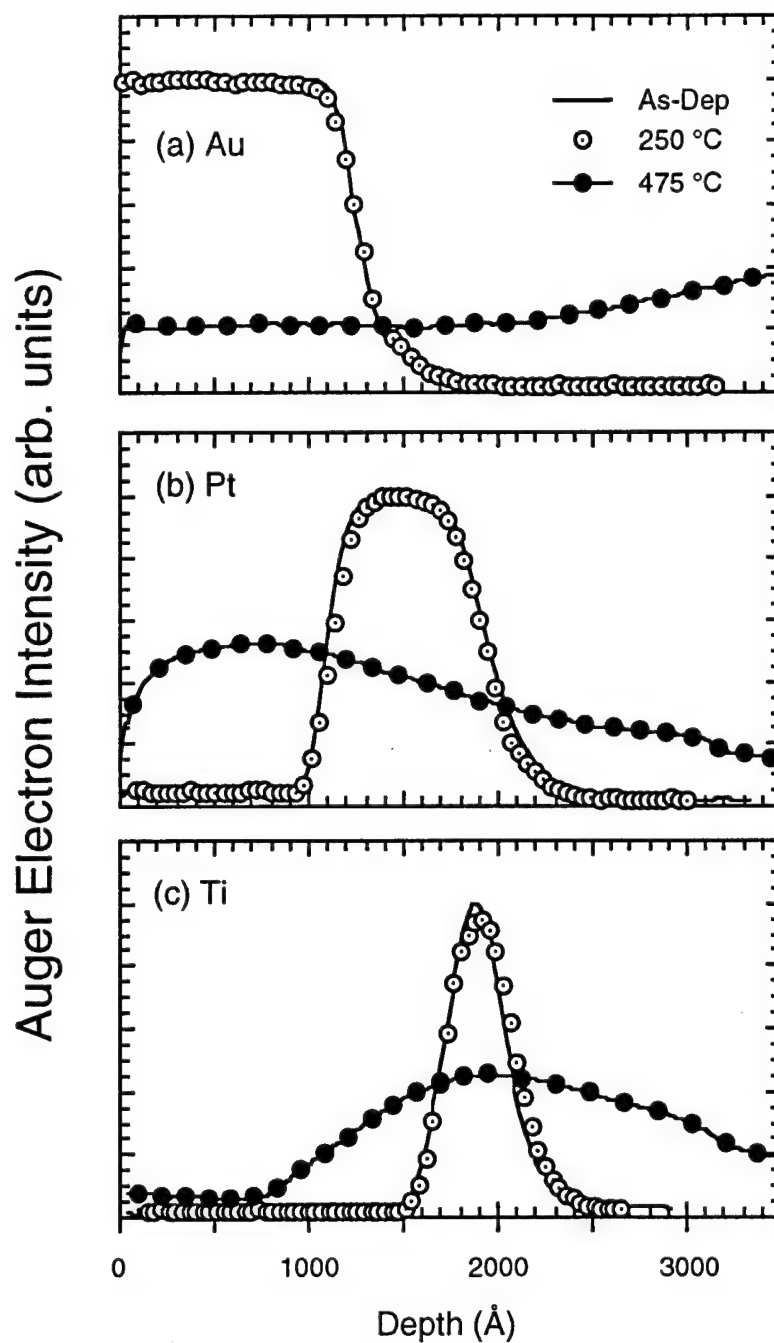


Figure 7.7. Auger electron spectroscopy depth profiles for Ti/Pt/Au (200/600/1000 Å) on Be-implanted GaAs_{0.46}Sb_{0.54}. The spectra were measured following deposition, and following RTA at T = 250 °C or 475 °C for 30 seconds. The (a) Au, (b) Pt, and (c) Ti depth profiles are shown.

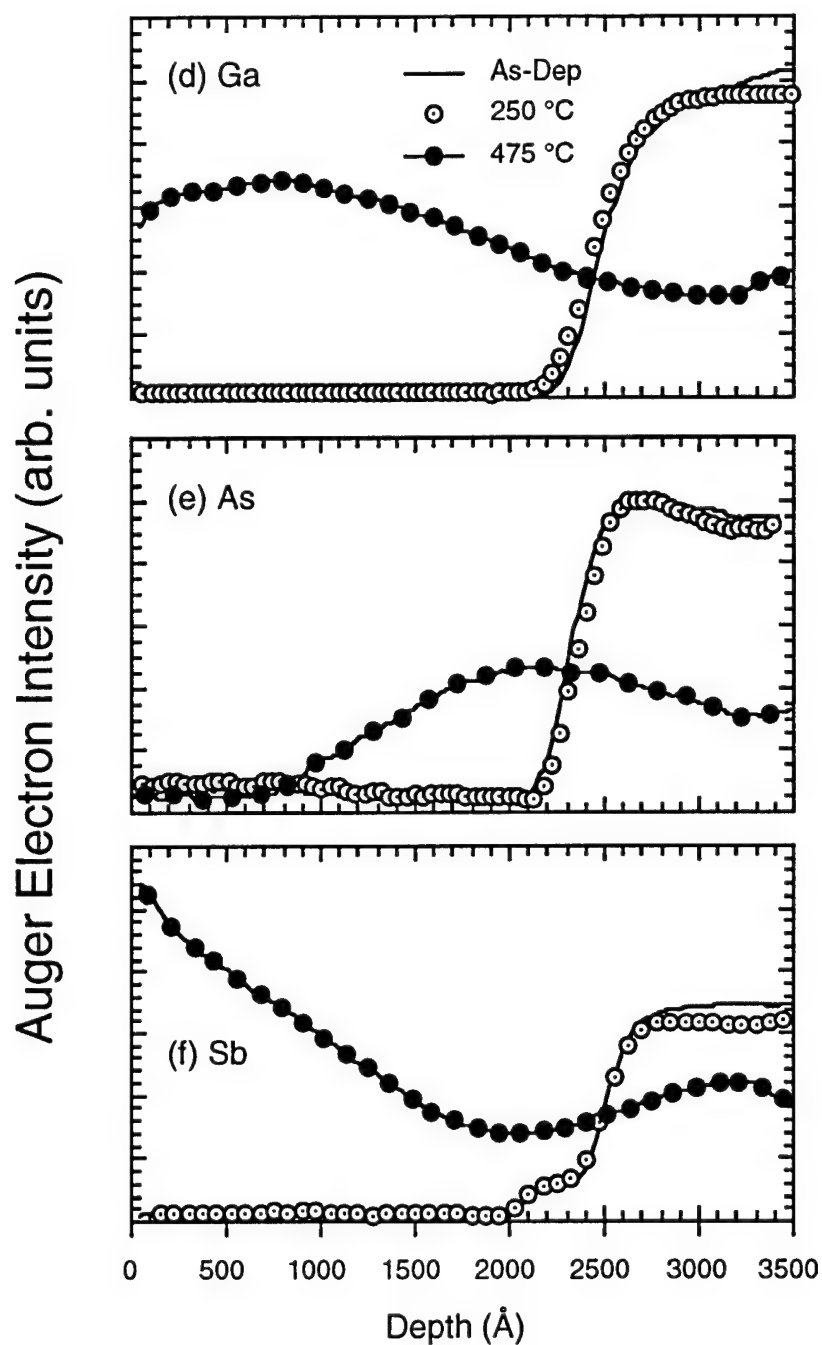


Figure 7.7 (cont.). Auger electron spectroscopy depth profiles for Ti/Pt/Au (200/600/1000 Å) on Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$. The spectra were measured following deposition, and following RTA at $T = 250\text{ }^{\circ}\text{C}$ or $475\text{ }^{\circ}\text{C}$ for 30 seconds. The (d) Ga, (e) As, and (f) Sb depth profiles are shown.

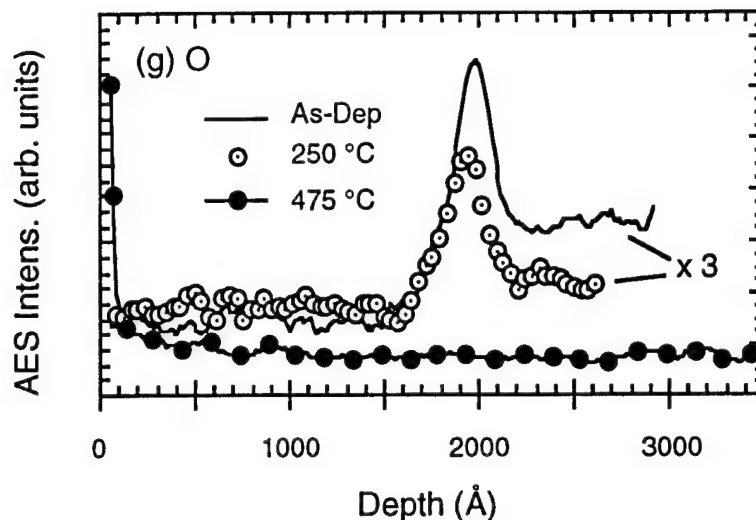


Figure 7.7 (cont.). Auger electron spectroscopy depth profiles for Ti/Pt/Au (200/600/1000 Å) on Be-implanted GaAs_{0.46}Sb_{0.54}. The spectra were measured following deposition, and following RTA at $T = 250\text{ }^{\circ}\text{C}$ or $475\text{ }^{\circ}\text{C}$ for 30 seconds. The (g) O depth profiles is shown. Intensities for the as-deposited and $T = 250\text{ }^{\circ}\text{C}$ case are expanded by a factor of 3 relative to the $T = 475\text{ }^{\circ}\text{C}$ case.

indicate breaching of GaAs_{0.46}Sb_{0.54} surface oxides upon sintering. These results demonstrate the metal/semiconductor interface remained intact after sintering at $T = 250\text{ }^{\circ}\text{C}$.

Considerable diffusion of all metal and semiconductor elements was detected after RTA at $T = 475\text{ }^{\circ}\text{C}$. A distinct metal-semiconductor interface was no longer observed. Gold diffused at least 3500 Å past the sample surface. Platinum and Ga outdiffused towards the surface. The Ga and Pt profiles were concurrent and had peak intensities in proximity at depths of 750 Å and 680 Å, respectively. Antimony outdiffused and congregated at the sample surface. This large amount of Sb may explain the greyish, metallic color of the Ti/Pt/Au sample surface following heating at $T = 475\text{ }^{\circ}\text{C}$. The Ti and As profiles were similar. Maxima for the Ti and As occurred at depths of 1950 Å and 2170 Å, respectively. AES thus detected the following regions proceeding from the sample surface: (1) Sb at the surface, (2) a Ga and Pt rich region centered around a depth of 700 Å, (3) a Ti and As rich region centered at a depth of 2100 Å, and (4) a Au rich region at a

depth of 3500 Å. Hence, complete degradation of the ohmic contact occurred at $T = 475$ °C.

7.4.3 X-Ray Diffraction and XTEM Results. X-ray diffraction (XRD), cross-sectional microscopy (XTEM), selected area diffraction (SAD) and energy dispersive X-ray analysis (EDX) were performed in order to determine microstructural interaction between the Ti, Pt, Au and GaAs_{0.46}Sb_{0.54} layers. XRD results are presented first in this section.

The XRD spectra for the Ti/Pt/Au samples are demonstrated in Figure 7.8. Diffraction peaks are labeled according to the element or compound identified by the ICDD Powder Diffraction File [Ch VI, Ref. 32]. The intensity scale was expanded to permit observation of low intensity peaks otherwise suppressed when plotted against the GaAs_{0.46}Sb_{0.54} peak. The spectra were taken following Ti/Pt/Au deposition, and after RTA at $T = 250$ °C and 475 °C for 30 seconds. The as-deposited spectrum exhibited diffraction peaks from the GaAsSb (or InP), Au and Pt layers. The GaAs_{0.46}Sb_{0.54} diffraction peak at 79.8° results from the {422} family of crystallographic planes. (The GaAs_{0.46}Sb_{0.54} diffraction peak was first identified from a XRD spectrum obtained from a sample with no metal layers.) The first three sets of Au and Pt diffraction peaks from left to right correspond to the {111}, {200} and {220} fcc planes. The Au layer is both thicker and lies above the Pt layer. Consequently, Au diffraction peaks are more intense than Pt peaks for these three crystallographic planes. The Au peaks correspond to a unit cell dimension of $a_0 = 4.077$ Å which is 0.04% below the ICDD value. Platinum peaks relate to a unit cell dimension of $a_0 = 3.911$ Å which is 0.31% below the ICDD value. Lack of diffraction from the Ti layer may result from: (1) an amorphous Ti layer, (2) the thin Ti layer (200 Å) having too low of a volume for detection, or (3) two potential Ti diffraction peaks at 38.4° {002} and 39.9° {101} overlapping with {111} peaks of Au and Pt at 38.2° and 40.1° , respectively. The XRD spectrum following RTA at $T = 250$ °C was essentially the same in terms of identified peaks and their diffraction angle. The

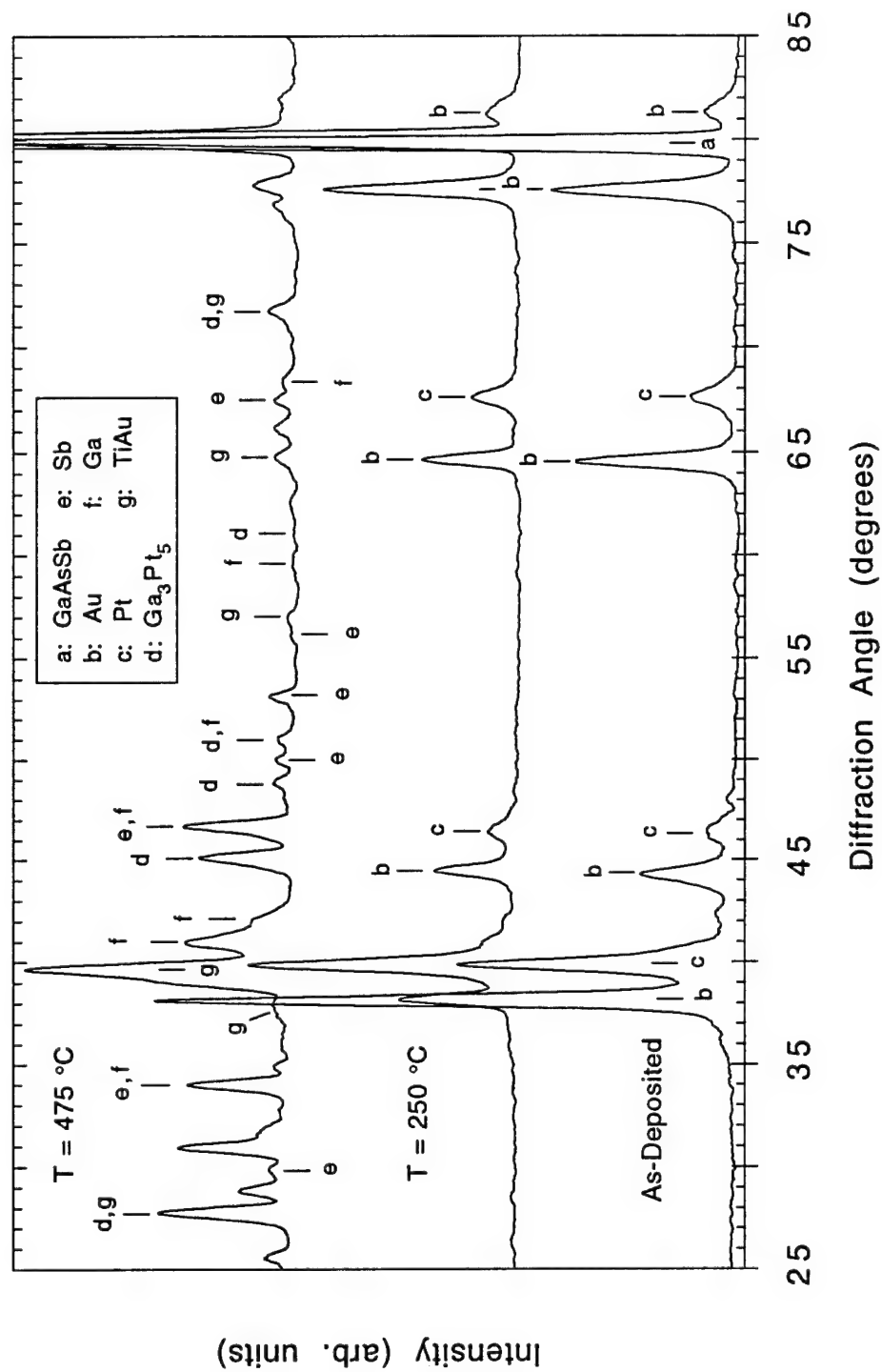


Figure 7.8 XRD spectra for Ti/Pt/Au (200/600/1000 Å) on $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ measured following metal deposition and RTA at 250 °C or 475 °C. Labeled peaks correspond to the phases identified in the inset.

sample subjected to RTA at $T = 475\text{ }^{\circ}\text{C}$ produced neither Au or Pt diffraction peaks. Numerous other peaks emerged, many of which were unassignable to diffraction standards.* Matches between diffraction peaks and standards were made with Ga_3Pt_5 , Sb, Ga and TiAu phases. These results demonstrate that no additional compounds are produced by sintering the Ti/Pt/Au ohmic contact at $T = 250\text{ }^{\circ}\text{C}$. However, RTA at $T = 475\text{ }^{\circ}\text{C}$ eliminates the Au and Pt layers, and produces binary compounds and elemental phases from the metal and semiconductor layers.

Following XRD, cross-sectional TEM, SAD and EDX characterization were performed on the three Ti/Pt/Au samples. Figures 7.9 through 7.11 display the XTEM and SAD results. EDX results are described in reference to microstructural regions contained in the XTEM micrographs.

Figures 7.9(a) and 7.9(b) respectively show the XTEM and SAD results, for the as-deposited Ti/Pt/Au sample. The Au, Pt, Ti, $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ and InP layers were easily identifiable in cross-section. The measured layer thicknesses for this region of the sample were Au - $1,200\text{ }\text{\AA}$, Pt - $580\text{ }\text{\AA}$, Ti - $200\text{ }\text{\AA}$, and $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ - $4700\text{ }\text{\AA}$. The Au layer was composed mostly of four-sided grains which varied approximately in longitudinal height as $230 \leq y \leq 1200\text{ }\text{\AA}$ and in latitude as $270 \leq x \leq 1800\text{ }\text{\AA}$. The Pt layer contained grains with smaller latitudinal dimensions (approximately $130 \leq x \leq 250\text{ }\text{\AA}$), and longitudinal grain boundaries extending through the entire layer. The Ti layer, exhibited no visible grain boundaries. No point or extended defects from growth, implantation or RTA were observed in the $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ layer. Only Au, Ti and Pt elemental peaks were observed in the EDX spectrum when the electron beam was placed approximately $200\text{ }\text{\AA}$ above the Au/Pt interface. The SAD pattern demonstrated ring patterns associated with the Au and Pt layers. Four sets of rings corresponding to the $\{111\}$, $\{200\}$, $\{220\}$ and $\{311\}$ crystallographic planes of Au and Pt were identified. No diffraction rings were measured

* Each diffraction spectrum was compared separately against 127 different diffraction standards representing all available combinations of Ti, Pt, Au, Ga, As, Sb and O.

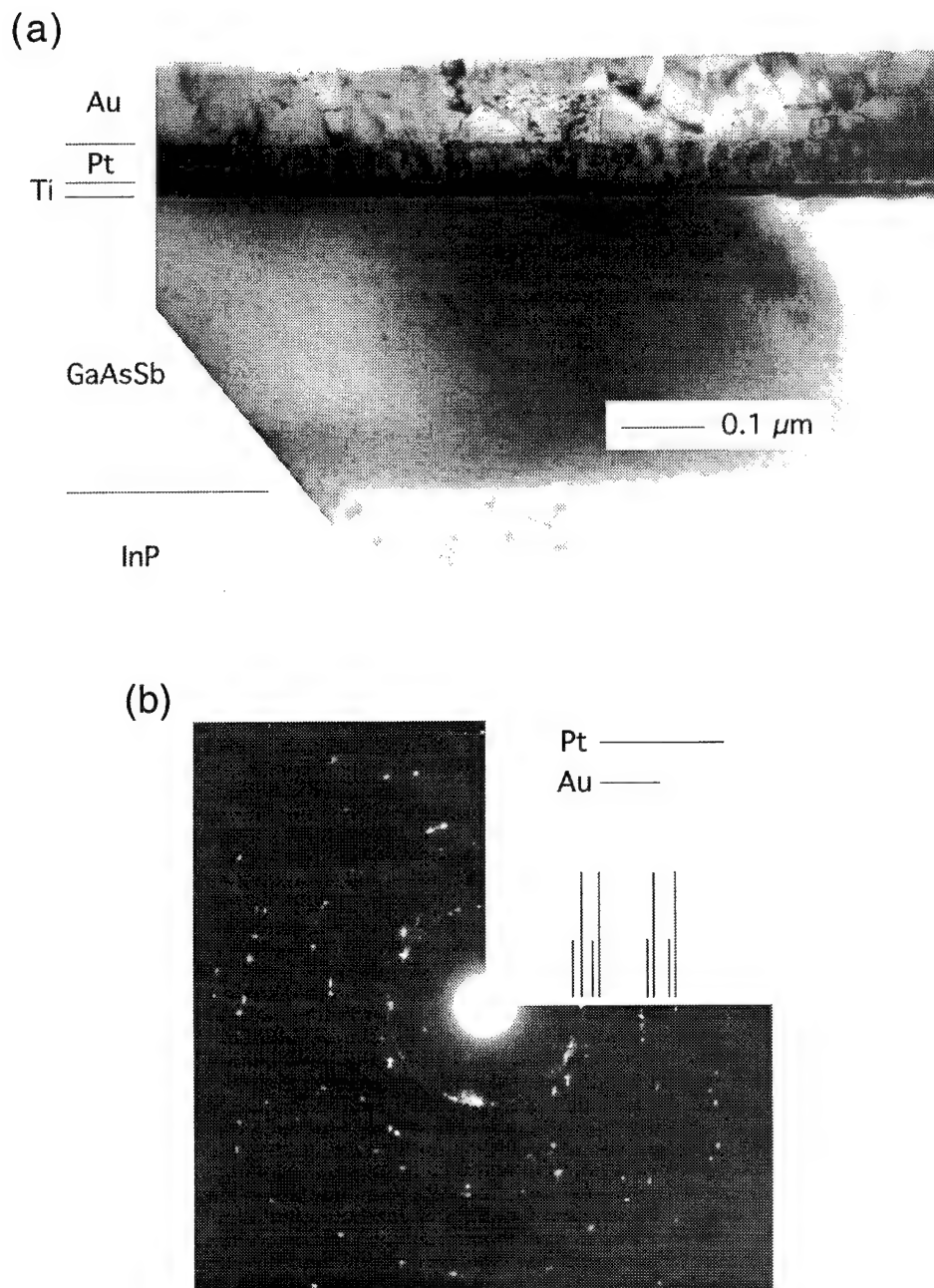


Figure 7.9. Transmission electron microscopy results for as-deposited Ti/Pt/Au (200/600/1000 Å) on Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$: (a) cross-sectional micrograph, and (b) selected area diffraction (SAD) pattern. One quadrant of the SAD pattern is eliminated to identify elemental diffraction rings. Long and short tick marks correspond to Pt and Au diffraction rings, respectively. The four sets of diffraction rings viewed from left to right result from the {111}, {200}, {220} and {311} family of planes.

for the Ti layer. These results indicate the as-deposited Ti layer is likely amorphous as per the lack of grain boundaries in the XTEM micrograph, the lack of XRD peaks and absence of SAD diffraction rings. Figure 7.9 shows the metallic layers are planar and well defined with no metal-semiconductor interactions appearing during deposition.

XTEM and SAD results, for the Ti/Pt/Au sample subjected to RTA at $T = 250\text{ }^{\circ}\text{C}$ are shown in Figures 7.10(a) and 7.10(b), respectively. The Au, Pt and Ti layers are again clearly identifiable. The Au layer was smoother with individual Au grains much less detectable when compared with the as-deposited micrograph. The Pt layer remained essentially the same after RTA at $T = 250\text{ }^{\circ}\text{C}$. A slight interfacial reaction between the Pt and Ti may have occurred as indicated by a continuous, light colored band between the two layers. EDX measurements again indicated only the Au, Pt and Ti elements. SAD characterization produced diffraction rings corresponding to the same Au and Pt crystallographic planes identified in the as-deposited sample. The Au SAD rings were less continuous and more intense than the as-deposited rings, reflecting an increase in the Au grain size after RTA at $T = 250\text{ }^{\circ}\text{C}$. These microstructural characterization results show the metal layers remain unreacted with $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ following RTA at $T = 250\text{ }^{\circ}\text{C}$.

Considerable degradation of the surface, and loss of metal and semiconductor layer integrity occurred after RTA at $T = 475\text{ }^{\circ}\text{C}$. Figure 7.11(a) and 7.11(b) demonstrate these reactions. The XTEM micrograph produced five distinct regions: (1) a very rough top layer varying between $1000\text{ }\text{\AA}$ and $2500\text{ }\text{\AA}$ in thickness, (2) a middle layer with a mostly uniform thickness of approximately $800\text{ }\text{\AA}$, (3) a bottom layer approximately $970\text{ }\text{\AA}$ thick, (4) spiked regions which extend roughly $1300\text{ }\text{\AA}$ past the bottom layer and (5) regions of $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ interspersed between the spiked regions. The maximum extent of the spiked region is approximately $5600\text{ }\text{\AA}$ below the sample surface. EDX analysis was taken in the center of each of the five regions. EDX demonstrated the following elements in each region: top layer - Au, Pt, Ga, Sb and As, middle layer - Au, Pt, Ga, As, Ti and Sb,

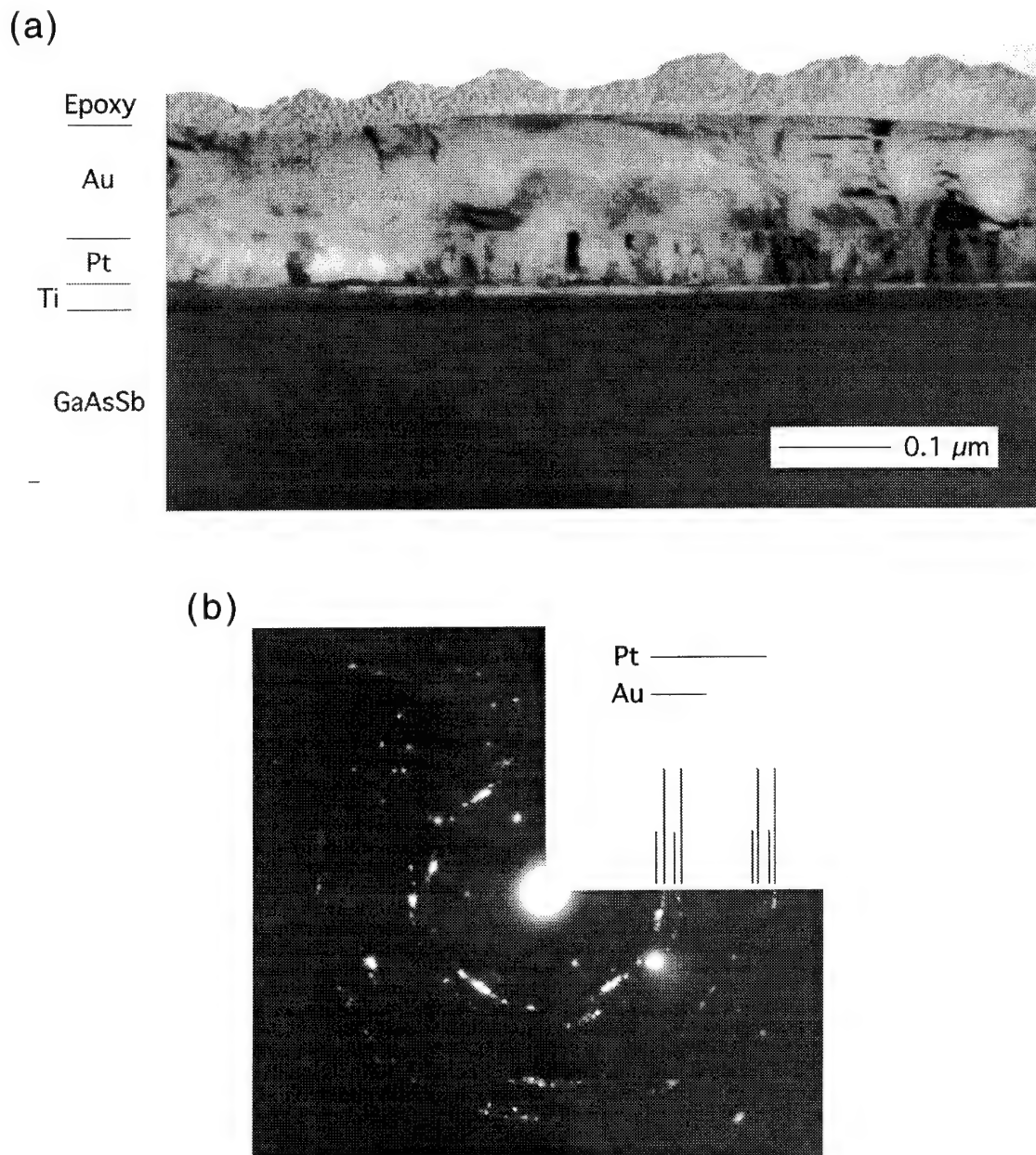
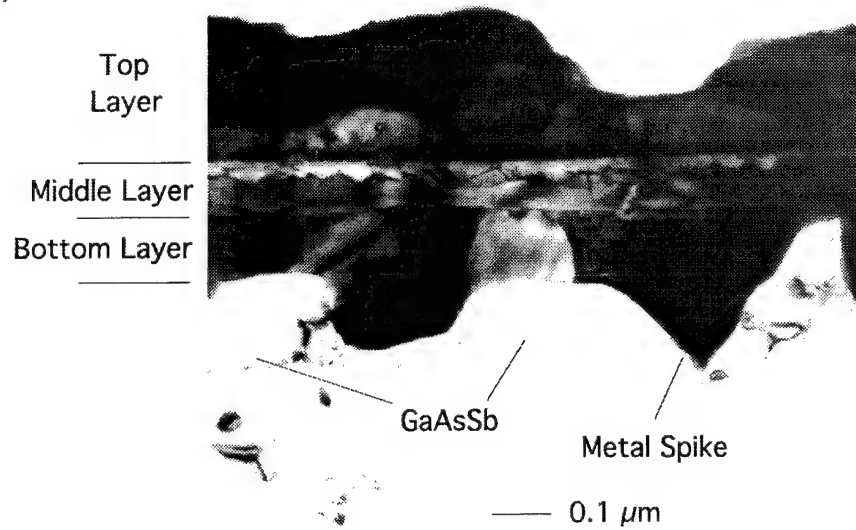


Figure 7.10 Transmission electron microscopy results for Ti/Pt/Au (200/600/1000 Å) on Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ following RTA at $T = 250^\circ\text{C}$ for 30 sec: (a) cross-sectional micrograph, and (b) selected area diffraction (SAD) pattern. One quadrant of the SAD pattern is eliminated to identify elemental diffraction rings. Long and short tick marks correspond to Pt and Au diffraction rings, respectively. The four sets of diffraction rings viewed from left to right result from the $\{111\}$, $\{200\}$, $\{220\}$ and $\{311\}$ family of planes.

(a)



(b)

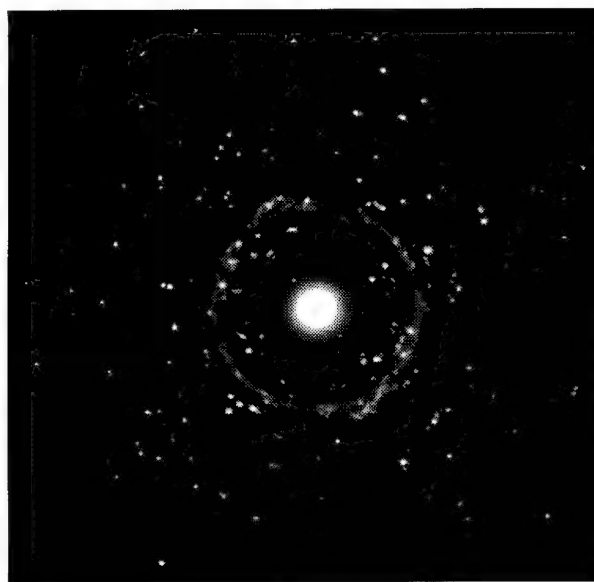


Figure 7.11 Transmission electron microscopy results for Ti/Pt/Au (200/600/1000 Å) on Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ following RTA at $T = 475^\circ\text{C}$ for 30 sec: (a) cross-sectional micrograph, and (b) selected area diffraction (SAD) pattern.

bottom layer - Pt, Au, Sb, As, and Ti, spiked region - Au, Pt, In, Sb, Ga, As and Ti. SAD ring patterns were too diffuse and the dot patterns were too numerous to identify individual phases in any region. This multiplicity of phases is demonstrated in the SAD micrograph of Figure 7.11(b) which was obtained from the center of the middle layer. The EDX results indicate Au has diffused at least 5000 Å past the sample surface. The In signal detected in the spiked region may result from In outdiffusion from the InP substrate or overlap of the electron beam with the substrate region. These results demonstrate that rapid thermal annealing of the Ti/Pt/Au contact at $T = 475\text{ }^{\circ}\text{C}$ produces nonuniform intermetallic diffusion deep into the $\text{GaAs}_{0.46}\text{Sb}_{0.54}$ epilayer.

7.5 InAlAs/GaAsSb HIGFET with Ti/Pt/Au Source and Drain Contacts

Previous sections of this chapter demonstrated very low contact resistance and excellent thermal stability for the Ti/Pt/Au ohmic contact at $T = 250\text{ }^{\circ}\text{C}$ on Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$. Consequently, Ti/Pt/Au is promising for device applications using Be-implanted, $\text{GaAs}_{1-x}\text{Sb}_x$, ohmic contact regions. However, a true test of the utility of an ion implant and ohmic contact combination requires demonstration of improved device performance based upon usage. This section demonstrates considerable improvement in the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET using Be ion implantation and Ti/Pt/Au nonalloyed source/drain contacts.

The $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET fabrication procedure is briefly described. Two $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET structures were epitaxially grown using MBE. Profile views of the two wafers are shown in Figure 7.12. The two structures differ only in the thickness of the undoped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ channel layer: 200 Å thick for wafer 842 and 150 Å for wafer 843. A 200 Å thick, Si-doped $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ layer is placed beneath the channel layer for threshold voltage control. Mesa formation and Be-implanted source/drain regions were obtained using the same fabrication steps as the

(a) InAlAs/GaAsSb HIGFET: 842

GaAs _{0.51} Sb _{0.49} :i, 50 Å
In _{0.52} Al _{0.48} As:i, 300 Å
GaAs _{0.51} Sb _{0.49} :i, 200 Å
In _{0.52} Al _{0.48} As:Si, N _D = 1 x 10 ¹⁷ cm ⁻³ , 200 Å
In _{0.52} Al _{0.48} As:i, 5000 Å
In _{0.52} Al _{0.48} As:i/In _{0.53} Ga _{0.47} As SL, 30/30 Å, 10 Periods
In _{0.52} Al _{0.48} As:i, 200 Å
Semi-Insulating InP Substrate

(b) InAlAs/GaAsSb HIGFET: 843

GaAs _{0.51} Sb _{0.49} :i, 50 Å
In _{0.52} Al _{0.48} As:i, 300 Å
GaAs _{0.51} Sb _{0.49} :i, 150 Å
In _{0.52} Al _{0.48} As:Si, N _D = 1 x 10 ¹⁷ cm ⁻³ , 200 Å
In _{0.52} Al _{0.48} As:i, 5000 Å
In _{0.52} Al _{0.48} As:i/In _{0.53} Ga _{0.47} As SL, 30/30 Å, 10 Periods
In _{0.52} Al _{0.48} As:i, 200 Å
Semi-Insulating InP Substrate

Figure 7.12. Layer profiles for In_{0.48}Al_{0.52}As/GaAs_{0.51}Sb_{0.49} HIGFETs: (a) wafer 842 and (b) wafer 843. The two wafers differ in GaAs_{0.51}Sb_{0.49} channel thickness.

TLM patterns described in Section 6.2. The Ti/Pt/Au layers on the source/drain regions were 200/600/3000 Å in thickness. Following metal deposition on the source/drain the Ti/Pt/Au contacts were subjected to RTA at $T = 250\text{ }^{\circ}\text{C}$ for 10 seconds. The gate region was next defined using a two step lithography process. The gate region was recessed using a dilute etch of $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O:L-Tartaric acid}$ (1:1:240:0.4) with an approximate etch rate of 5 Å/s in $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ and 2.5 Å/s in $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$. An etch depth 25 Å into the 300 Å thick, $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ gate layer was targeted. Following the recess etch Ti/Pt/Au (200/600/3000 Å) was deposited as the gate metallization. Therefore, a single metallization scheme was used for the source, drain and gate contacts. The following discussion focuses on DC electrical measurement results for HIGFETs obtained from wafers 842 and 843. Prominent aspects are provided for large scale devices (gate length, $L_G = 1\text{ }\mu\text{m}$, gate width, $W_G = 200\text{ }\mu\text{m}$) and small scale devices ($L_G = 1\text{ }\mu\text{m}$, $W_G = 10\text{ }\mu\text{m}$).

Figures 7.13(a) and 7.13(b) show the family of drain-to-source current versus voltage curves (I_{DS} vs V_{DS}), extrinsic transconductance, g_{me} , and square root of drain-source current, $(I_{DS})^{1/2}$, for a large scale device on wafer 843. Wafer 843 produced the best large scale devices in terms of maximum current capability and linear region I-V characteristics. Figure 7.13(a) shows the I-V curves. The saturated source-drain current, I_{DSS} , was maximum at $|I_{DSS}| \geq 1.2\text{ mA}$ when $V_{GS} = -2.0\text{ V}$. The drain-source saturation current stepped uniformly with respect to V_{GS} . These uniform current steps indicate superior control of the channel current by the gate voltage. The voltage onset for drain-source breakdown was large for these devices, occurring at $V_{DS} \cong -12\text{ V}$. The gate-source threshold voltage was $V_{GS} = V_{tp} = 0.17\text{ V}$ as shown by: (1) the reduction in I_{DS} to zero current at this gate bias as in Figure 7.13(a), and (2) extrapolation of the $(I_{DS})^{1/2}$ curve to zero in Figure 7.13(b). Hence, the HIGFET is operating as an enhancement mode device due to the normally off state. The maximum g_{me} for this device was 3.5 mS/mm. The largest measured external transconductance obtained on wafer 843 was $g_{me} = 5.1\text{ mS/mm}$.

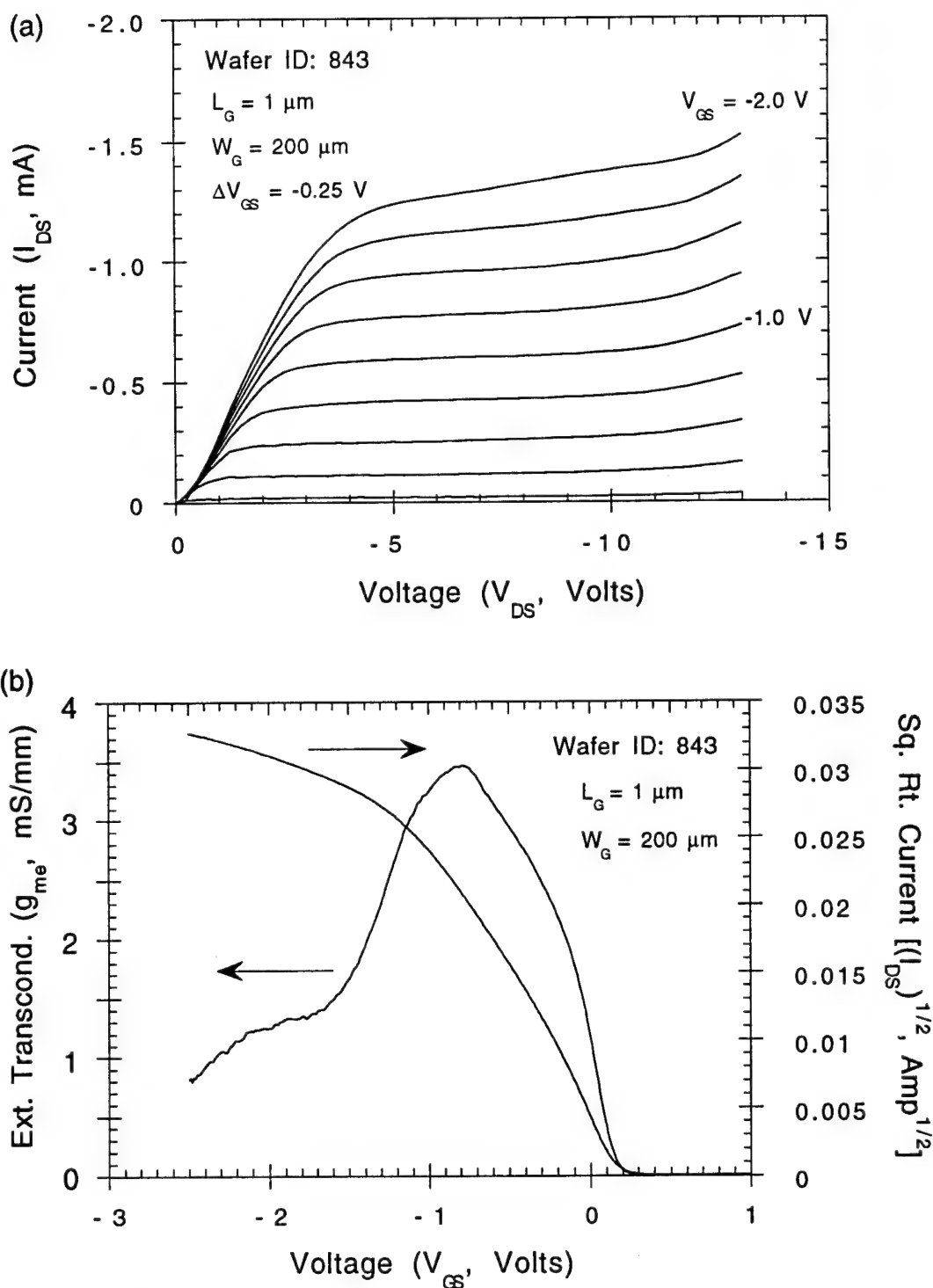


Figure 7.13. DC electrical characteristics of an $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET: (a) family of I_{DS} vs V_{DS} curves, and (b) extrinsic transconductance, g_{me} , and square root of I_{DS} versus gate-source voltage, V_{GS} . The gate dimensions are $1 \mu\text{m} \times 200 \mu\text{m}$.

However, the linear and saturation region characteristics of this device were not as good as those in Figure 7.13(a).

Figure 7.14 shows another set of I-V curves for a large scale device from wafer 843. This device had a less resistive linear region and improved current handling capacity compared to the HIGFET of the previous figure. The saturated source-drain current was maximum at $|I_{DSS}| \geq 2.0$ mA when $V_{GS} = -2.0$ V. This value was the maximum channel current measured on either of the two wafers. Again, the drain-source saturation current stepped uniformly with respect to V_{GS} . Figures 7.13 and 7.14 indicate the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET is robust in terms of current handling capability and breakdown voltage. These are desirable characteristics when considering analog circuit applications.

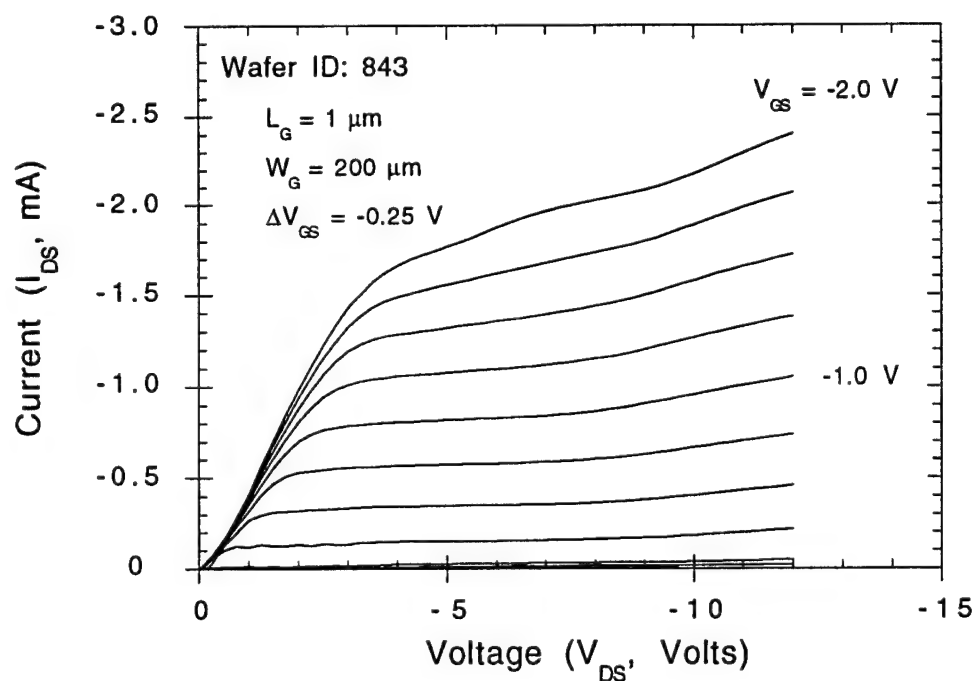


Figure 7.14. Family of I_{DS} vs V_{DS} curves for an $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. This device demonstrated the largest saturated source-drain current with $|I_{DSS}| \geq 2.0$ mA. The gate dimensions are $1 \mu\text{m} \times 200 \mu\text{m}$.

Current-voltage curves for small scale devices are shown in Figures 7.15 and 7.16. The curves were obtained from wafer 842. Figure 7.15 illustrates a highly linear I-V characteristic in the linear region of the family of curves. The saturation region exhibited a low output conductance with saturation currents as large as $|I_{DSS}| = 52 \mu\text{A}$. Also, the device in Figure 7.15 did not breakdown with application of a drain-source voltage as large as $V_{DS} = -10 \text{ V}$ indicating. Figure 7.16 shows the maximum measured current on a small scale device. In this case, $|I_{DSS}| \geq 80 \mu\text{A}$ for $V_{GS} = -2.5 \text{ V}$. The channel saturation current stepped uniformly with respect to V_{GS} on the small devices. External transconductances measured on the small devices were $g_{me} \leq 5 \text{ mS/mm}$.

These results demonstrate Be-implantation and Ti/Pt/Au contact metallization serve as a complete combination for formation of the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. A comparative analysis of these electrical results is deferred until the next section.

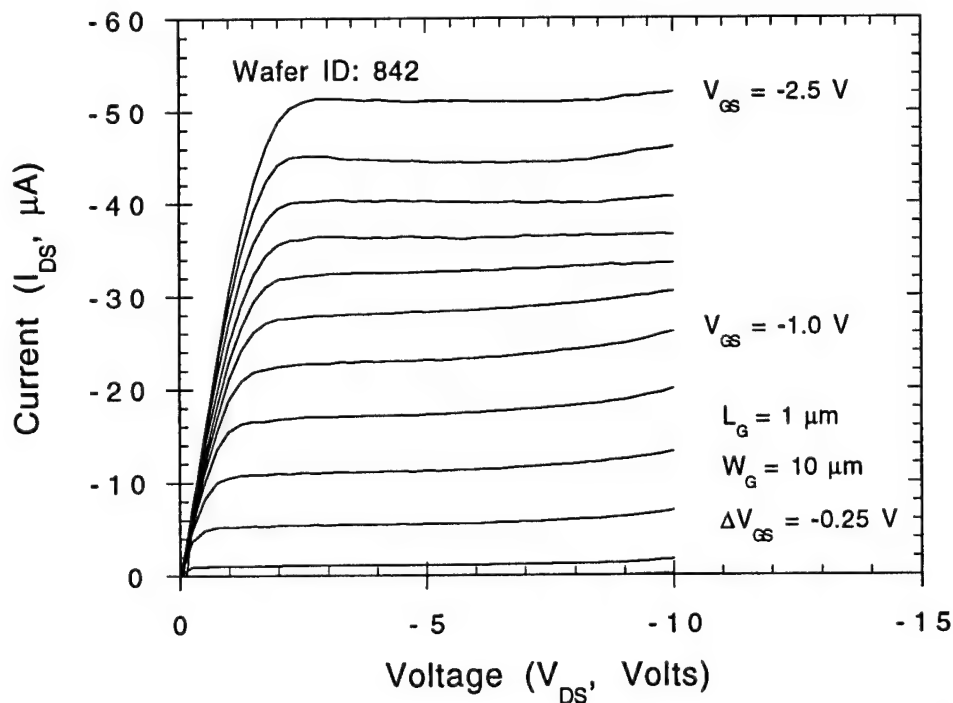


Figure 7.15. Family of I_{DS} vs V_{DS} curves for an $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. This device demonstrated the best linear region characteristics and lowest output conductance for a small geometry device. The gate dimensions are $1 \mu\text{m} \times 10 \mu\text{m}$.

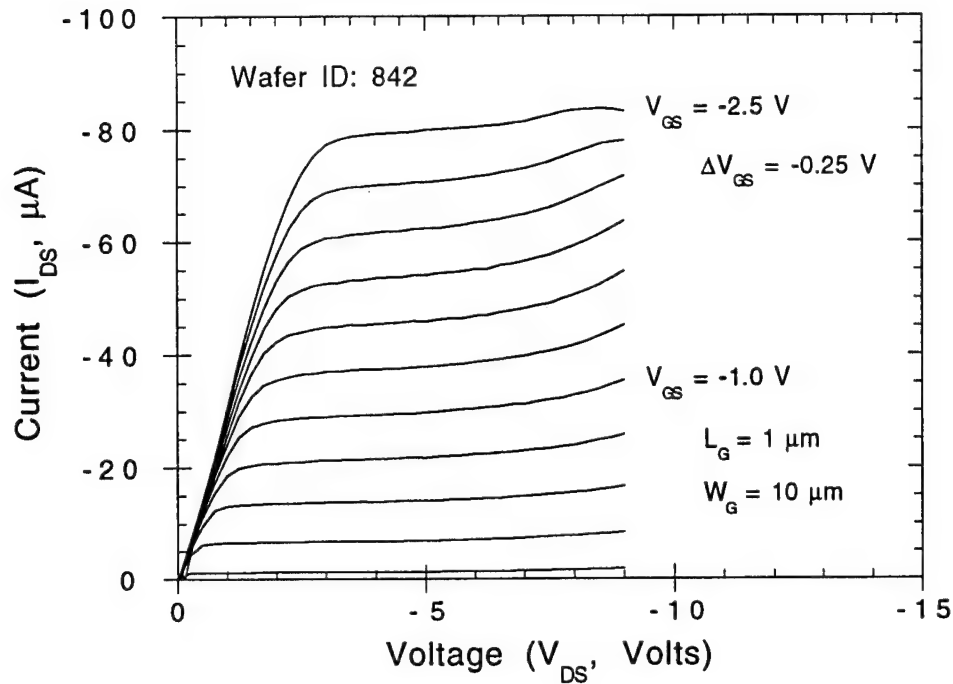


Figure 7.16. Family of I_{DS} vs V_{DS} curves for an $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. This device demonstrated the largest saturated source-drain current with $|I_{DSS}| \geq 80 \mu\text{A}$. The gate dimensions are $1 \mu\text{m} \times 10 \mu\text{m}$.

7.6. Discussion of Experimental Results

7.6.1 Discussion of Ti/Pt/Au Ohmic Contact Results. In this section the results of electrical and microstructural characterization of the Ti/Pt/Au ohmic contact are analyzed. Correlations between the TLM and microstructural characterization results are highlighted. Also, emphasized are consistencies between the different microstructural characterization methods.

A comparison of Figures 7.1 through 7.3 yields conclusions concerning the electrical performance of the Ti/Pt/Au ohmic contact. First, extremely low contact resistance is achievable using this metal/semiconductor system. RTA at $T = 250^\circ\text{C}$ produces a minimum value of contact resistance $R_C = 0.021 \Omega\text{-mm}$ ($\rho_C = 1.82 \times 10^{-8} \Omega\text{-cm}^2$). This value is well below the benchmark design value of $R_C = 0.1 \Omega\text{-mm}$ ($\rho_C = 1.0 \times$

$10^{-6} \Omega\text{-cm}^2$) as outlined in Section 2.2. Two factors directly contribute to this low contact resistance: (1) the high surface acceptor concentration afforded by Be ion implantation ($N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$), and (2) the relatively narrow direct bandgap energy of $\text{GaAs}_{1-x}\text{Sb}_x$ at or near lattice matched to InP ($E_g = 0.74 \text{ eV}$ for $x = 0.49$). Second, a minimal dependence on RTA time is apparent for the Ti/Pt/Au ohmic contact. The contact resistance was minimized with an RTA cycle as short as $t = 5$ seconds at $T = 250^\circ\text{C}$. This short RTA cycle is advantageous in cases where sequential batch processing of devices is required. Third, thermal stability appears excellent at $T = 250^\circ\text{C}$ since $R_c \leq 0.1 \Omega\text{-mm}$ for up to 500 hours. Finally, in all TLM measurements, the $\text{GaAs}_{1-x}\text{Sb}_x$ sheet resistance remained essentially constant with RTA temperature and time, or thermal storage time. This constancy implies no lateral penetration into the semiconductor by the Ti/Pt/Au during these measurements.

Reduction in contact resistance with a 250°C thermal cycle is most likely accomplished through penetration of an oxide barrier versus a metal-semiconductor interaction. Comparison of TLM thermal measurements, AES, XTEM and XRD results verifies this assertion. TLM thermal measurements indicated a very small metal-semiconductor hole barrier height on the as-deposited sample, $\phi_{BP} = 0.022 \text{ eV}$. This same barrier height was measured on the Au/Zn/Au samples of Section 6.3.2. Therefore, the barrier height is independent of metallization type - an indication of Fermi level pinning. Acceptor concentrations of $N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$ would produce a degenerate semiconductor layer with tunneling as a predominant conduction mechanism in the absence of an interfacial oxide layer.* TLM thermal measurements summarized in Table 7.1 show no tunneling component for the as-deposited contacts with conduction occurring over the small barrier. After thermal cycling at $T = 250^\circ\text{C}$ a parallel, tunneling conduction path emerges along with the same thermionic, interfacial barrier height. Therefore, the interfacial

* Figure 2.9(b) theoretically demonstrates that hole transport across a metal- $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ interface occurs through field emission when the barrier height is less than 0.2 eV .

electrical characteristics remained the same in the thermionic area of the contact. AES results demonstrated an interfacial oxide following Ti/Pt/Au deposition as per Figure 7.7(g). RTA at $T = 250\text{ }^{\circ}\text{C}$ reduced the oxygen content, while further heating to $T = 475\text{ }^{\circ}\text{C}$ eliminated the oxide layer. The AES results also indicated slight penetration of this oxide layer by the Ti after the $250\text{ }^{\circ}\text{C}$ RTA. XTEM demonstrated no interpenetration of metal and semiconductor layers following RTA at $T = 250\text{ }^{\circ}\text{C}$. Also, XRD and SAD measurements established no additional phase formation. These results indicate Ti diffusion through the oxide layer reduces contact resistance at $T = 250\text{ }^{\circ}\text{C}$ without formation of intermetallic or metal-semiconductor phases. TLM thermal probe measurements show the diffusion is nonuniform and occurs over approximately 14 % of the contact area.

Conclusions concerning surface morphology with respect to RTA temperature are warranted. AFM, XTEM and SAD results concur on Au surface morphology following RTA at $T = 250\text{ }^{\circ}\text{C}$. AFM measurements established an increase in the Au grain size diameter by a factor of four from the $0.023 - 0.061\text{ }\mu\text{m}$ size range measured as-deposited. The increase in grain size was concurrent with a reduction in Au surface roughness. XTEM micrographs and SAD also indicated larger grain size. Loss of continuity in SAD diffraction rings with increased intensity of diffraction spots establishes increased grain size. Thus multiple benefits are derived from RTA at $T = 250\text{ }^{\circ}\text{C}$ - minimized contact resistance, smoother contact surfaces, and a Au layer with increased crystalline uniformity. Smoother contact surfaces assist deposition of planarized overlay metals. Loss of grain boundaries and increased uniformity of the Au layer improves current flow uniformity, assists sub-micron dimensional scaling, and should improve device reliability due to reduced potential for electromigration at grain boundaries [9].

Thermal degradation of the Ti/Pt/Au ohmic contact at $T = 475\text{ }^{\circ}\text{C}$ appears linked to a few different processes. Complete loss of distinct metal and semiconductor regions

occurred at this temperature. XTEM micrographs delineated four different regions in the sample. The top layer was very nonuniform at the surface and was rich in Sb, Ga and Pt. Surface nonuniformity was apparent in both XTEM and AFM micrographs. The XTEM micrograph of Figure 7.11 demonstrated a peak-to-valley roughness of approximately 1500 Å along the sample surface. AFM measured a peak-to-valley roughness of approximately 6000 Å over a 1 µm x 1 µm scan area. AES spectra showed an excess of Sb at the surface. Antimony diffraction peaks were also observed in the XRD spectra. Beneath the Sb-rich surface a layer rich in Ga and Pt was detected by AES. Both Ga₃Pt₅ and Ga phases appear to form in this region as per XRD results. EDX also detected Sb, Ga and Pt in this layer. Consequently, the top layer is composed of Sb, Ga and Pt. The top layer is Sb-rich at its surface with a (Ga,Pt)-rich region near the layer bottom. Antimony outdiffusion may be prompted by an initial accumulation of Sb at the GaAs_{0.46}Sb_{0.54} surface following ion implantation. SIMS results of Figures 5.16(c) and 5.17(c) show loss of Ga and As following Be-implantation and annealing with no Sb loss. Correspondingly, the AES results of Figure 7.7(f) show an Sb-rich layer between the as-deposited Ti and GaAs_{0.46}Sb_{0.54} layers. The middle layer is rich in Ti and As as per AES and EDX results. XRD detected no compounds containing Ti and As. However, TiAu diffraction peaks were measured by XRD. AES demonstrated Au diffusion through the middle layer while Au was detected by EDX as well. Therefore, the Au concentration seems dense enough to form TiAu. The bottom layer and spiked regions are rich in Au as per EDX measurements. Deep indiffusion of Au is therefore a distinct failure mechanism. AES results showed a reduction in the Au profile at the sample surface. This indiffusion was observed optically by transition in sample surface coloration from gold to a greyish metallic color. Loss of surface Au was also demonstrated by the lack of Au XRD peaks following the high temperature cycle. In summary, microstructural characterization results dictate morphological degradation and increased contact resistance are caused by: (1) loss of metal

layer integrity due to deep indiffusion of Au, and (2) loss of semiconductor layer integrity due to outdiffusion of Sb and Ga.

These experimental results verify a low resistance ohmic contact is produced through the application of Ti/Pt/Au to Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$. This Ti/Pt/Au contact is quite superior to Au/Zn/Au in terms of thermal stability and should suffice for any device which employs p-type $\text{GaAs}_{1-x}\text{Sb}_x$ epilayers on InP.

7.6.2 Discussion of HIGFET Results. The above experimental results on the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET must be balanced against reported progress for other p-HIGFET designs. In this section, the experimental results are compared first against $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFETs [10,11]. Secondly, other III-V material systems are compared, including $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ [12-19], $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}$ [20], and $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ [21-23].

The most direct proof of device improvement using Be-implantation and Ti/Pt/Au source/drain metallization is obtained through comparison with prior results on the recessed-gate, lattice-matched, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET [10]. This process used a 500 Å thick, Be-doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer for a source/drain cap layer [cf. Figure 4.1(b)]. Electrical access to the channel was obtained through diffusion of Au/Zn/Au source/drain contacts through the $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer at $T = 250^\circ\text{C}$. These devices were fabricated with the same mask set used in Section 7.5. Therefore, direct comparison of results is valid. The maximum extrinsic transconductance achieved on large scale ($1\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$) devices was $g_{me} = 1.4\text{ mS/mm}$. The maximum saturated current obtained was $|I_{DSS}| = 0.4\text{ mA}$. The drain-source saturation current stepped very nonuniformly with respect to V_{GS} . Complete cutoff of the channel was not obtained under any bias condition. The channel thickness was $t = 250\text{ Å}$ (compared with $t = 150\text{ Å}$ for wafer 843) and the channel was Be-doped with $N_A = 4 \times 10^{17}\text{ cm}^{-3}$ (versus nominally undoped for wafer 843). By comparison, the Be-implanted HIGFET with Ti/Pt/Au

metallization produced a g_{me} which was 2-3 times higher with a five fold increase in maximum I_{DSS} . Uniform steps in I_{DSS} as well as complete channel cutoff were achieved as per Figures 7.13 - 7.16. These improvements were realized even though a reduced channel thickness and lower channel doping were employed compared to the recessed gate, Au/Zn/Au HIGFET design. These improvements in the g_{me} and I_{DSS} performance of lattice matched HIGFETs are attributed to reduced source/drain resistance provided by low contact resistance and a low resistance current path to the channel through the Be implanted regions.

Improved device performance is also inherent from observations of surface morphology and device yield considerations. M.J. Martinez made a general observation concerning the Au/Zn/Au contact on the InAlAs/GaAsSb HIGFET:

“Problems with the alloyed contacts severely limited yield of these devices. Most of the transistors on the wafers behaved as short circuits, indicating an excess of lateral diffusion during contact alloy. A closer examination during fabrication revealed that while contact resistance was very uniform prior to the anneal step, this uniformity was lost after anneal. There can be no doubt that, to be manufacturable, the devices will require a more repeatable and uniform ohmic contact [10].”

Diffusive surface layers such as those observed in Martinez's work [10] and Chapter VI of this document would interject leakage paths to the gate and reduce device yields due to shorting between neighboring electrodes. Removal of leakage paths would improve gate control of the channel. Improved gate control is apparent in Figures 7.13 - 7.16. Unlike the recessed gate HIGFETs with Au/Zn/Au source/drain contacts, the majority of the $1\text{ }\mu\text{m}$ x $200\text{ }\mu\text{m}$ HIGFETs on wafer 843 produced working transistors with linear I-V regions, and definite channel cutoff. No diffusive surface layers were observed on any of the transistors following the $T = 250\text{ }^{\circ}\text{C}$ source/drain contact sinter. Considerable

improvements in both the I-V characteristics and thermal reliability of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET were thus demonstrated using Be implantation and Ti/Pt/Au contact metallization.

Additional improvements in $\text{In}_y\text{Al}_{1-y}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET performance are foreseen with respect to uniformity, yield, and gain. Optimizing the gate recess etch, incorporating strained layer channels, and adjusting the under channel doping density should raise g_{me} . A 25 Å recess etch into the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ gate layer was used for HIGFETS in Figures 7.13 - 7.16. Increasing the etch depth should improve the ability of the gate to modulate channel conduction and consequently increase g_{me} . Additional channel doping and increased uniformity in the source/drain implant most likely will improve the linear region of these devices. Lattice matched channels serve as a platform for judging the impact of HIGFET design schemes without the additional variable of strained layer effects. Strained channel layers of $\text{GaAs}_{0.35}\text{Sb}_{0.65}$ have produced the best performance for $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ -based p-HIGFETs [11]. The strained channel layer is believed to increase hole mobility by simultaneously reducing alloy scattering and decoupling the heavy and light hole valence bands. These devices were fabricated using the recessed gate configuration and Au/Zn/Au ohmic contacts [11]. Extrinsic transconductances as high as $g_{me} = 40 \text{ mS/mm}$ were measured on devices with gate geometries of $1 \mu\text{m} \times 200 \mu\text{m}$. Applying Be-implanted source/drain regions with Ti/Pt/Au metallization should additionally enhance the good performance of $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFETs with strained layer channels.

$\text{GaAs}_{1-x}\text{Sb}_x$ -based ($x \leq 0.15$) p-HIGFETs with $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ gate layers suffer from poor cutoff characteristics or low transconductance. The $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}_{0.85}\text{Sb}_{0.15}$ HIGFET ($50 \mu\text{m} \times 400 \mu\text{m}$) produced $g_{me} = 0.3 \text{ mS/mm}$ without complete channel cutoff [12]. Increased transconductance was obtained on HIGFETs with the same epilayers and reduced gate dimensions ($1 \mu\text{m} \times 20 \mu\text{m}$), $g_{me} =$

12.5 mS/mm [13]. However, channel cutoff was never completely obtained. Early p-HIGFET designs employed the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ heterojunction. Maximum extrinsic transconductances as high as $g_{me} = 55$ mS/mm were measured [19]. Yet, channel cutoff was incomplete [14-18] unless devices were cooled to $T = 77$ K [14,19] or an implanted n-well was used [18]. These results demonstrated that hole confinement inside the valence band discontinuity was inadequate when $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ was used in conjunction with $\text{GaAs}_{1-x}\text{Sb}_x$ ($x \leq 0.15$).

Employing $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ as the gate layer improves hole confinement and p-HIGFET device performance on InP substrates. HIGFETs employing the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ heterojunction with $1.2 \mu\text{m} \times 20 \mu\text{m}$ gate dimensions achieved maximum extrinsic transconductances of $g_{me} = 33$ mS/mm [13]. The I-V characteristics demonstrated attainable device cutoff, uniform steps in I_{DSS} with respect to gate voltage steps, and low output conductance. However, the linear region of the I-V curves demonstrated an offset voltage at $I_{DS} = 0$. These offset voltages are produced by an additional voltage drop across the source resistance when high gate bias causes source-to-gate conduction [24]. In this device design AuZn was deposited on Be-implanted $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ to form the source and drain contacts.

The $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ p-HIGFET has yielded the top performance in terms of transconductance and process maturity. Peak extrinsic transconductances of $g_{me} = 113$ mS/mm were realized on $0.8 \mu\text{m} \times 10 \mu\text{m}$ devices using $\text{Al}_{0.47}\text{Ga}_{0.53}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ [21]. Device cutoff appeared lacking when $|V_{DS}| \geq 2.0$ V, however. These improved devices are believed caused by superior hole confinement due to an increased gate layer bandgap energy due to increased Al mole fraction ($x > 0.3$). Complementary $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ HIGFETs are currently produced in a manufacturing product line at Motorola to produce a variety of IC designs [22]. Maximum extrinsic transconductances of $g_{me} = 60$ mS/mm were measured on p-HIGFET devices with $1 \mu\text{m} \times$

10 μm gate dimensions. Modified device designs using the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ heterojunction in tandem with a graded, n^+ $\text{In}_y\text{Ga}_{1-y}\text{As}$ ($0 \leq y \leq 0.5$) gate cap layer were reported [23]. These devices produced a maximum extrinsic transconductance of $g_{\text{me}} = 50 \text{ mS/mm}$. Devices with $1 \mu\text{m} \times 50 \mu\text{m}$ gate geometries demonstrated a high frequency performance of $f_t = 5 \text{ GHz}$.

Summary comments are evident following comparison of the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET with respect to alternate heterojunction technologies. The addition of Be-implanted source/drain regions with nonalloyed Ti/Pt/Au ohmic contacts definitely improves the device yield and thermal reliability of the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET compared to recessed gate designs using Au/Zn/Au. These improvements will permit accurate evaluation of HIGFET designs employing modifications to epilayers and device geometries. Beryllium ion implantation and Ti/Pt/Au source/drain contacts applied to strained layer $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFETs will permit optimization of these heterojunction devices as well. Strained layer $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFETs appear to face the greatest challenge from the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ HIGFET. Some of the fundamental deciding factors between these two device technologies are gate layer performance and process maturity.

Gate layer performance. Heterojunction hole confinement and gate layer barrier height for $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ versus $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ begets comparison. Superior hole confinement in the channel appears evident for the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET [11, Section 7.5] versus the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ p-HIGFET [21,23]. Comparison of I-V curves demonstrates a more direct channel cutoff for the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET at higher drain-source biases ($|V_{\text{DS}}| \geq 2\text{V}$). The large valence band discontinuity for $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ is a major contributing factor. A comparison of valence band offsets shows $\Delta E_v = 0.72 \text{ eV}$ for $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.35}\text{Sb}_{0.65}$ [11] versus $\Delta E_v = 0.4 \text{ eV}$ for $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$

[25]. A larger hole barrier height exists for $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$ ($\phi_{\text{BP}} = 1.6 \text{ eV}$ [23]) versus $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ ($\phi_{\text{BP}} = 0.9 \text{ eV}$ [10]). The higher ϕ_{BP} may produce the lower subthreshold leakage currents measured on $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ HIGFETs.

Process maturity. Considerable improvement in $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET device process is necessary in order to compete with $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ devices in terms of yield and process maturity. Production of an n-HIGFET in the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ remains necessary while complementary HIGFETs are available in the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ system. The use of GaAs versus InP substrates is also more attractive for the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ HIGFET due to lower cost, larger available substrate diameters, and the larger number of additional electronic and optoelectronic devices available on GaAs substrates for co-integration. Epilayers and fabrication techniques were more complex for the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ HIGFET than the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ devices reported thus far. These included graded n-type gate layers, AlAs and GaAs spacer layers and two p-type source/drain implants. Increased effort on heterojunction materials and device fabrication processes should considerably improve $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET performance and permit a more direct comparison with $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ HIGFET technologies.

7.7 Chapter VII Summary

The Ti/Pt/Au metallization scheme produces an extremely low contact resistance ($R_c < 0.09 \text{ } \Omega\text{-mm}$; $\rho_c < 3 \times 10^{-7} \text{ } \Omega\text{-cm}^2$) on Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$. This contact is thermally stable at $T = 250 \text{ }^\circ\text{C}$ for up to 500 hours and can withstand thermal cycling to $T = 450 \text{ }^\circ\text{C}$. Thermal degradation of the contact at $T = 475 \text{ }^\circ\text{C}$ is caused by simultaneous Au indiffusion and Ga and Sb outdiffusion. Employment of Ti/Pt/Au as a source, drain and gate metallization produces a single, conventional metallization for the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. HIGFET performance is improved with

respect to, ohmic contact reliability, external transconductance, maximum current capability, output conductance and FET cutoff characteristics. This implantation and metallization combination will directly enhance future designs, including submicrometer, SAG $\text{In}_y\text{Al}_{1-y}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFETs with strained channel layers.

Chapter VII Bibliography

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VIII. Conclusions and Future Research

The experimental results of the previous chapters are summarized in Section 8.1. Opportunities for expanded research on the $\text{GaAs}_{1-x}\text{Sb}_x$ semiconductor and the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET are outlined in Section 8.2.

8.1 Conclusions

This dissertation produced the first ion implanted $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET, and improved the source and drain contacts. To the authors knowledge, each experimental task represented a "first" with respect to the $\text{GaAs}_{1-x}\text{Sb}_x$ semiconductor and the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET. These first efforts include: (1) evaluating the thermal stability of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET, (2) determining the temperature dependence of E_g and impurity energy levels in $\text{GaAs}_{0.51}\text{Sb}_{0.49}$, (3) ion implantation of $\text{GaAs}_{1-x}\text{Sb}_x$ on InP, (4) microstructural and electrical characterization of Au/Zn/Au and Ti/Pt/Au on $\text{GaAs}_{1-x}\text{Sb}_x$, (5) producing an ion implanted $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET with a single metallization for the three electrodes.

Temperature limits for the SAG $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET were determined. This research delineated the thermal limitations of: (1) beryllium-implanted $\text{GaAs}_{1-x}\text{Sb}_x$, (2) $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET epilayers, and (3) two ohmic contacts on $\text{GaAs}_{1-x}\text{Sb}_x$. The Be implantation studies of Chapter V demonstrate a dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and a 10 second, 600 °C RTA produces the least amount of damage to the Si_3N_4 and the greatest amount of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface stability. Results in Chapter IV show SAG HIGFET epilayers are intact to 600 °C. SAG epilayer degradation initiates at 700 °C and is total at 800 °C. Therefore, 600 °C is the upper thermal limit imposed on the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ SAG HIGFET due to the stability requirements of

HIGFET epilayers and the implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ surface. The maximum temperature achieved before ohmic contact degradation was $T \leq 250^\circ\text{C}$ for Au/Zn/Au and $T \leq 450^\circ\text{C}$ for Ti/Pt/Au on $\text{GaAs}_{1-x}\text{Sb}_x$. Consequently, HIGFETs should not be subjected to temperatures above 400°C once Ti/Pt/Au source and drain contacts are deposited. Study of the thermal reliability of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ with optimized epilayer configurations and Ti/Pt/Au metallization is a next, logical study.

Chapter IV experimentally determined the thermal stability of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ HIGFET was dependent on $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ cap layer thickness. Thermal stability was maintained to $T = 700^\circ\text{C}$ by a recessed-gate structure using a 500 \AA cap layer and $T = 600^\circ\text{C}$ for a SAG structure with a 50 \AA cap layer. Epilayer degradation appears related to the capacity of elements to outdiffuse into the cap layer and mass at the sample surface. The thinner 50 \AA cap layer, more readily allows outdiffusing elements to mass at the surface at 700°C than does the 500 \AA cap layer. Degradation is produced by outdiffusion of In and Al from the gate layer and loss of Ga from the cap layer. Indium, Al and Sb mass at the surface in circular regions at $T = 700^\circ\text{C}$ in the SAG structure. The 500 \AA cap layer accommodates larger concentrations of outdiffusing elements than the 50 \AA cap layer. Therefore, outdiffusion of In occurs from deep within the RG structure at $T = 800^\circ\text{C}$.

Optical characterization of Be-doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ permitted determination of E_g and donor and acceptor energy levels as functions of ambient temperature. The temperature dependence of E_g followed the Varshni relationship with coefficients $\alpha = 13.5 \times 10^{-4}\text{ eV/K}$, $\beta = 135\text{ K}$ and $E_g(0) = 0.814\text{ eV}$. Two acceptor energy levels were observed - one residual and one Be-related. The residual acceptor has an ionization energy of $E_A = 12\text{ meV}$. The Be-related acceptor level is 31 meV below the residual acceptor level for $2 \leq T \leq 10\text{ K}$. These energy relationships are applicable in future efforts involving characterization and modeling of $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ -based systems.

This dissertation demonstrated the ability to achieve high acceptor concentrations in p-type $\text{GaAs}_{1-x}\text{Sb}_x$ on InP using Be ion implantation. Acceptor concentrations of $N_A \geq 1 \times 10^{19} \text{ cm}^{-3}$ were obtained within 1000 Å of the $\text{GaAs}_{1-x}\text{Sb}_x$ surface. This doping density was realized by implanting through a 1000 Å Si_3N_4 cap layer under the following conditions: $E = 50 \text{ keV}$, $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ or $1 \times 10^{15} \text{ cm}^{-2}$, and $\theta = 7^\circ$. Implant activation is limited by Ga back sputtering, and Ga and As outdiffusion from the $\text{GaAs}_{1-x}\text{Sb}_x$ surface during RTA. The Ga and As-related reactions are implant dosage and RTA temperature dependent - back sputtering increases with increasing dose; outdiffusion increases with increasing RTA temperature. Therefore, increasing the dose to $Q_0 = 1 \times 10^{15} \text{ cm}^{-2}$ increases the acceptor concentration at the expense of decreased surface stability. Hall effect measurements of Section 6.3.3 demonstrate Be implant activation percentages as high as 94 % in $\text{GaAs}_{1-x}\text{Sb}_x$ when $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ and RTA is accomplished at $T = 600^\circ\text{C}$. Phenomenological modeling of the mobility indicates the predominant scattering mechanism is alloy scattering at room temperature. Therefore, applying a Be dose of $Q_0 = 5 \times 10^{14} \text{ cm}^{-2}$ with subsequent RTA at $T = 600^\circ\text{C}$ produces the best compromise between acceptor concentration and surface stability. This dose/temperature combination was selected for ohmic contact layers. The Be implantation study yielded highly doped $\text{GaAs}_{1-x}\text{Sb}_x$ layers which successfully produced low resistance, nonalloyed ohmic contacts.

The results of Chapters VI and VII permit comparison of Au/Zn/Au and Ti/Pt/Au as ohmic contacts to Be-implanted $\text{GaAs}_{1-x}\text{Sb}_x$ on InP. A degradatory reaction between Au and Sb provides a fundamental impediment to obtaining a Au-based ohmic contact to $\text{GaAs}_{1-x}\text{Sb}_x$. This reaction was observed initially on Au/Zn/Au contacts to epitaxially doped $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ at $T = 250^\circ\text{C}$ [1]. Chapter VI demonstrated the Au-Sb reaction occurs in Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ at temperatures as low as $T \approx 100^\circ\text{C}$. TLM measurements show a reduction in Au/Zn/Au contact resistance following RTA at $T = 250^\circ\text{C}$. However, AES and XTEM results show that Au-Sb degradation reaction is prevalent at $T = 250^\circ\text{C}$. At $T = 325^\circ\text{C}$ the following occur: deep indiffusion of Au, outdiffusion and

clustering of Sb at the sample surface, and the formation of AuSb₂. Loss of surface Ga and As during implantation and annealing potentially exacerbates the Au-Sb reaction relative to unimplanted GaAs_{0.51}Sb_{0.49} layers. Therefore, direct application of Au to GaAs_{1-x}Sb_x must be avoided in an electrical contact to Be-implanted GaAs_{0.51}Sb_{0.49}.

The electrical performance of the Ti/Pt/Au contact was superior to the Au/Zn/Au contact. Electrical and microstructural characterization show Ti/Pt/Au contact resistance is minimized and structural integrity improved by sintering at $T = 250\text{ }^{\circ}\text{C}$ for 30 seconds. A minimum average contact resistance of $R_c = 0.01\text{ }\Omega\text{-mm}$ was obtained for Ti/PtAu on GaAs_{0.46}Sb_{0.54} following RTA at $T = 250\text{ }^{\circ}\text{C}$ for 30 seconds. This reduction in R_c at $T = 250\text{ }^{\circ}\text{C}$ is achieved with thermal cycles as short as 5 seconds. XTEM, XRD and AES results demonstrate no interpenetration of the metal-semiconductor interface at $T = 250\text{ }^{\circ}\text{C}$. Improvement in contact resistance at $T = 250\text{ }^{\circ}\text{C}$ is therefore believed to result from Ti penetration through GaAs_{0.46}Sb_{0.54} surface oxides as shown in AES spectra. Oxide penetration is further validated in TLM thermal probe measurements. A thermionic emission region of the Ti/Pt/Au contact with a barrier height of $\phi_{BP} = 0.022\text{ eV}$ was measured following deposition and RTA up to temperatures of $T = 250\text{ }^{\circ}\text{C}$. Following the $250\text{ }^{\circ}\text{C}$ sinter, a field emission region emerges over 14 % of the effective contact area while the thermionic region barrier height remains the same. Emergence of a field emission region following sintering is indicative of partial metal penetration through the surface oxide to the highly doped GaAs_{0.46}Sb_{0.54} surface. AFM, XTEM and SAD measurements demonstrated improvement in the Au surface morphology following the $250\text{ }^{\circ}\text{C}$ sinter. The Au surface roughness was reduced and Au grain size increased. Other positive observations for the Ti/Pt/Au contact include $R_c \leq 0.05\text{ }\Omega\text{-mm}$ after 500 hours of thermal storage at $T = 250\text{ }^{\circ}\text{C}$. The Ti/Pt/Au contact remained intact to $T = 450\text{ }^{\circ}\text{C}$ with the average $R_c \leq 0.1\text{ }\Omega\text{-mm}$ (and $\rho_c \leq 1 \times 10^{-6}\text{ }\Omega\text{-cm}^2$). Following RTA at $T = 475\text{ }^{\circ}\text{C}$ the contact is thoroughly degraded due to: deep indiffusion of Au, outdiffusion and clustering of Sb at the sample surface, and the formation of Ga₃Pt₅. Two conclusions thus emerge from

microstructural and electrical studies of the Ti/Pt/Au contact on Be-implanted $\text{GaAs}_{0.46}\text{Sb}_{0.54}$: (1) the 600 Å Pt layer behaves as a sufficient barrier to Au indiffusion and Sb outdiffusion at temperatures below 400 °C, and (2) sintering at $T = 250$ °C provides extremely low contact resistance and improves surface morphology. This ohmic contact experiment dictated use of Ti/Pt/Au as a nonalloyed ohmic contact to the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET.

Chapter VII demonstrated the advantages of using Ti/Pt/Au and Be-implanted source and drain regions on the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. Ti/Pt/Au produces a single, conventional metallization for the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET. HIGFET reliability was improved over previous Au/Zn/Au designs which exhibited shorting between the gate and other electrodes upon alloying. Ion implanted source and drain regions and the low specific contact resistance contributed to an increase in the external transconductance from 1.4 mS/mm to 5.1 mS/mm and the maximum saturated drain current increased from 400 µA to 2 mA. The low output conductance and superior cutoff characteristics of the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ p-HIGFET relative to other III-V designs were thus verified.

8.2 Future Research

Chapter V was an extensive study of Be ion implantation in $\text{GaAs}_{1-x}\text{Sb}_x$. The study was designed to obtain surface acceptor concentrations suitable for ohmic contact formation. Additional efforts to optimize the implant and anneal conditions are warranted. Five additional tasks are worth addressing:

(1) Reduction of the implant dosage and RTA temperature. Reduction of the Be dosage to $Q_0 = 3 \times 10^{14} \text{ cm}^{-2}$ should reduce implant damage and enable a higher activation percentage. Figure 5.1 theoretically indicates that surface acceptor concentrations between $6 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ are possible using this lower dosage. Reduction of the implant dosage may enable implant activation at RTA temperatures below 600 °C RTA.

These results would improve both the $\text{GaAs}_{1-x}\text{Sb}_x$ surface stability and HIGFET epilayer integrity.

(2) Model statistical profiles for a GaAsSb implant library. Ion implantation modeling programs often rely on experimental data to generate theoretical profiles. Statistical descriptions of Be implant profiles in $\text{GaAs}_{1-x}\text{Sb}_x$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ would assist in device design. Statistical parameters such as range, straggle, skew and kurtosis could be fitted numerically to experimental profile data. Implant dose, energy, and incident angle and Sb composition would be useful parameters for variation.

(3) Expand the available implant species for GaAsSb. Little research has focused on potential dopant species for $\text{GaAs}_{1-x}\text{Sb}_x$. To the author's knowledge, this dissertation represents the first effort to dope $\text{GaAs}_{1-x}\text{Sb}_x$ using ion implantation. $\text{GaAs}_{1-x}\text{Sb}_x$ is unique in terms of its doping properties. Early research on LPE-grown $\text{GaAs}_{1-x}\text{Sb}_x$ obtained n-type doping using Te and p-type doping using Ge for $x \leq 0.2$ [2]. Tin behaves amphoterically: p-type for $x \leq 0.14$ and n-type for $x \geq 0.18$ [3]. A comprehensive study of epitaxial doping and ion implantation using various elemental species would be beneficial. A useful study would investigate Si and C doping as a function of Sb composition since these are conventional dopants for $\text{Al}_{1-x}\text{Ga}_x\text{As}$.

(4) Investigate ion implantation in the GaAsSb/InAlAs heterojunction. This is a daunting (but necessary) task due to limitations in profile characterization and modeling. An electrochemical etchant applicable to both $\text{GaAs}_{1-x}\text{Sb}_x$ and $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ is currently unavailable. Therefore, obtaining the activated carrier concentration profile will require a multilayer etchant. Another issue is detecting Be accumulation at the heterojunction interface during implantation and annealing.

(5) Examine lateral diffusion of the implanted species. Sub-micron SAG designs must accommodate lateral straggle of dopants from the implanted source/drain. The extent of lateral diffusion could be characterized experimentally or modeled theoretically. A test structure similar to a TLM structure may suffice for experimental characterization. This

structure would have implantation only underneath the metallization with varying spacing between implanted regions. Following implantation and RTA, metal would be applied to the implanted regions. The allowed lateral separation between implanted regions is then detected by electrical shorting across nominally unimplanted segments of semiconductor. Such a test structure could determine the permissible source-to-gate spacing for SAG designs. A two-dimensional profile model would also establish implant parameters prior to actual implantation. One such model is currently under development at the University of Texas for 2-D profile modeling in Si [4].

Effective mass is a very important parameter for modeling and simulation. Electron and hole effective masses were approximated in this dissertation in order to accomplish: (i) theoretical calculations of specific contact resistance of a metal contact to $\text{GaAs}_{1-x}\text{Sb}_x$ (Section 2.1), (ii) modeling of the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{0.51}\text{Sb}_{0.49}$ SQW (Section 4.4), and (iii) phenomenological modeling of the hole mobility in Be-implanted $\text{GaAs}_{0.51}\text{Sb}_{0.49}$ (Section 6.3.3). Experimental measurement of these parameters as a function of impurity concentration, temperature and Sb composition would greatly assist future modeling and simulation efforts.

A number of prospective R&D efforts for the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET are logical. Chapter VII demonstrated improved performance of the p-channel $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET. The p-HIGFET device needs optimization in parallel with development of an n-channel device. An ultimate goal is a SAG, strained layer, complementary technology. Variations in the epilayer design and process improvements will ultimately enhance the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ p-HIGFET over current designs. The remaining paragraphs outline necessary research efforts for advancement of the HIGFET.

Optimization of the gate recess should improve device gain. Once the optimum recess depth into the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ is determined, the 300 Å gate layer thickness may be reduced by a corresponding amount. Then the recess etch is only required through the 50

Å GaAs_{0.51}Sb_{0.49} cap layer. The source/drain resistance would be reduced by thinning the wide band gap gate layer.

The advantages of channel strain should be thoroughly examined for n- and p-HIGFETs. Strained layer designs with $x = 0.65$ have thus far provided the best gain performance for the p-channel device. Improved performance of the In_{0.48}Al_{0.52}As/GaAs_{1-x}Sb_x HIGFET is envisioned when the Sb composition in the channel is raised above the lattice matched composition, $x \geq 0.49$. Both carrier confinement and channel mobility should be improved. Increasing the Sb composition lowers the channel bandgap energy and potentially increases carrier confinement by increasing ΔE_c and ΔE_v . Raising the Sb composition raises the light hole energy level relative to the heavy hole and should improve channel hole mobility due to enhanced conduction of light holes [5]. Mobility improvements should also occur due to reduction in alloy scattering which is maximum close to the lattice matched condition. Theoretical models exist for calculating heterojunction band offset energies due to strain [5]. Strained layer designs could be evaluated using the theoretical band offsets in theoretical models which simulate HFET operation [6]. The ability to vary the channel Sb composition is ultimately limited by critical thickness considerations for the In_{0.48}Al_{0.52}As/GaAs_{1-x}Sb_x heterojunction. Figure 5.21 serves as a guide for the critical thickness of the GaAs_{1-x}Sb_x channel.

Superior hole confinement in the In_{0.48}Al_{0.52}As/GaAs_{0.51}Sb_{0.49} HIGFET was again verified in Section 7.5 by the low output conductance and excellent cutoff characteristics. The advantages of superior hole confinement due to the large ΔE_v may be offset by poor electron confinement since $\Delta E_c = 0.1\Delta E_v$. Figure 4.13 graphically displays the disparity between ΔE_c and ΔE_v . Strained layer channels may decrease the inequity between the valence and conduction band discontinuities. Experimental designs should include band edge discontinuity measurements for each Sb composition studied since these discontinuities are needed for device modeling and heterojunction evaluation.

Device uniformity and yield are a bane of III-V devices relative to Si. These problems must be detected and corrected early in the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET development cycle by using whole wafer characterization. Characterization of epilayer compositional uniformity using whole wafer XRD is a useful pursuit. As of this writing, reports concerning MBE growth of $\text{GaAs}_{1-x}\text{Sb}_x$ have used only 2" diameter InP substrates. Mapping of defects in InP substrates and as-grown wafers will assist advancement of this technology to larger diameter substrates. The results of composition and defect mapping are feedback parameters for HIGFET wafer growth. Test reticules on mask sets must accommodate material and electrical characterization. Reliability testing of fully fabricated n- and p-channel devices is also needed. These reliability tests should include thermal, electrical and radiation stressing in environments which mirror operating conditions.

In conclusion, the p-channel $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET has demonstrated initial promise for application in a complementary III-V FET technology. This research effort has advanced the thermal stability of the electrical interface to the source and drain regions of the p-HIGFET. Also, progress was made towards a simple self-aligned gate design by combining ion implantation with a single device metallization. Numerous opportunities exist for continued exploration of the $\text{GaAs}_{1-x}\text{Sb}_x$ semiconductor and the $\text{In}_{0.48}\text{Al}_{0.52}\text{As}/\text{GaAs}_{1-x}\text{Sb}_x$ HIGFET.

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Captain Ken Merkel was born on 23 Sep 1960 in St Louis, Missouri. He enlisted in the Air Force in 1980. He served as a Precision Measurement Equipment Specialist from 1981 to 1983 at Maxwell AFB, Alabama. He entered the Airman Education and Commissioning Program in 1984. He was awarded a Bachelor of Science in Electrical Engineering from the University of Nebraska - Lincoln in 1986. He was commissioned a second lieutenant through Officer Training School in 1987. In 1988, he was awarded the Master of Science in Electrical Engineering (MSEE) under a NASA fellowship at the University of Nebraska - Lincoln. His MSEE research involved characterization of GaAs/AlGaAs superlattices and heterojunctions using variable-angle spectroscopic ellipsometry. Captain Merkel was next assigned to the Wright Laboratory, Solid State Electronics Directorate at Wright Patterson AFB, Ohio from 1988 to 1992. He specialized in the fabrication of GaAs/AlGaAs and InAlAs/GaAsSb heterojunction bipolar transistors, refractory ohmic contacts, and photoluminescence characterization of GaAs/AlGaAs quantum wells. He became a PhD candidate in Electrical Engineering at the Air Force Institute of Technology in 1992. He has authored 19 publications in the field of III-V materials and devices. Capt Merkel is a member of the Tau Beta Pi and Eta Kappa Nu engineering honorary societies. He is also a member of IEEE, and the Air Force Association.

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- S1. K.G. Merkel, C.L.A. Cerny, V.M. Bright, F.L. Schuermeyer, T. Monahan, R.T. Lareau, R. Kaspi and A.K. Rai, "Improved P-Channel InAlAs/GaAsSb HIGFET Using Ti/Pt/Au Ohmic Contacts to Beryllium Implanted GaAsSb", submitted to *Solid-State Electronics*, Jul 1995.
- S2. K.G. Merkel, V.M. Bright, C.L.A. Cerny, F.L. Schuermeyer, J.S. Solomon and R. Kaspi, "Beryllium Ion Implantation in GaAsSb Epilayers on InP", submitted to *J. Appl. Phys.*, Jun 1995.
- S3. C.L.A. Cerny, K.G. Merkel, F.L. Schuermeyer, V.M. Bright and R. Kaspi, "P-Channel, Ion Implanted, GaAsSb/InAlAs HIGFETs on InP for Digital and Microwave Applications", to be published in the IEEE Cornell Conference Proceedings (to be presented at the IEEE/Cornell University Conference on Advanced Concepts in High Speed Semiconductor Devices, 7-9 Aug 1995).
- 1. K.G. Merkel, C.L.A. Cerny, R.T. Lareau, V.M. Bright, P.W. Yu and F.L. Schuermeyer, "Rapid Thermal Annealing Effects on the Structural Integrity of InAlAs/GaAsSb HIGFET Epilayers on InP", *Compound Semiconductors 1994*, (Presented at the 21st Int'l Symp. on Compound Semiconductors, San Diego CA, 18-22 Sep 1994) pp. 727-732, 1995.

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